Digital Controller for Isolated Power Supply Applications

ADP1043

FEATURES

- **Integrates all typical controller functions**
  - **Digital control loop**
  - **Remote and local voltage sense**
  - **Primary and secondary side current sense**
  - **PWM control**
  - **Synchronous rectifier control**
  - **Current sharing**
  - **Integrated programmable loop filter**
- **I²C interface**
- **Extensive fault detection and protection**
- **Extensive programming**
- **Fast calibration**
- **EEPROM**
- **Standalone or microcontroller control**

APPLICATIONS

- **AC-to-DC power supplies**
- **Isolated dc-to-dc power supplies**
- **Redundant power supplies**
- **Parallel power supplies**
- **Server, storage, network, and communications infrastructure**

GENERAL DESCRIPTION

The ADP1043 is a secondary side power supply controller IC that is designed to provide all the functions that are typically needed in an isolated ac-to-dc or dc-to-dc control application.

The ADP1043 is optimized for minimal component count, maximum flexibility, and minimum design time. Features include remote voltage sense, local voltage sense, primary and secondary side current sense, pulse-width modulation (PWM) generation, and hot-swap sense and control. The control loop is digital with an integrated programmable digital filter. Protection features include current limiting, undervoltage lockout (UVLO), and overvoltage protection (OVP).

The built-in EEPROM provides extensive programming of the integrated loop filter, PWM signal timing, inrush current, and soft start timing and sequencing. Reliability is improved through a built-in checksum and redundancy of critical circuits.

A comprehensive GUI is provided for easy design of loop filter characteristics and programming of the safety features. The industry-standard I²C bus provides access to the many monitoring and system test functions.

The ADP1043 is available in a 32-lead LFCSP and operates from a single 3.3 V supply.

TYPICAL APPLICATION CIRCUIT

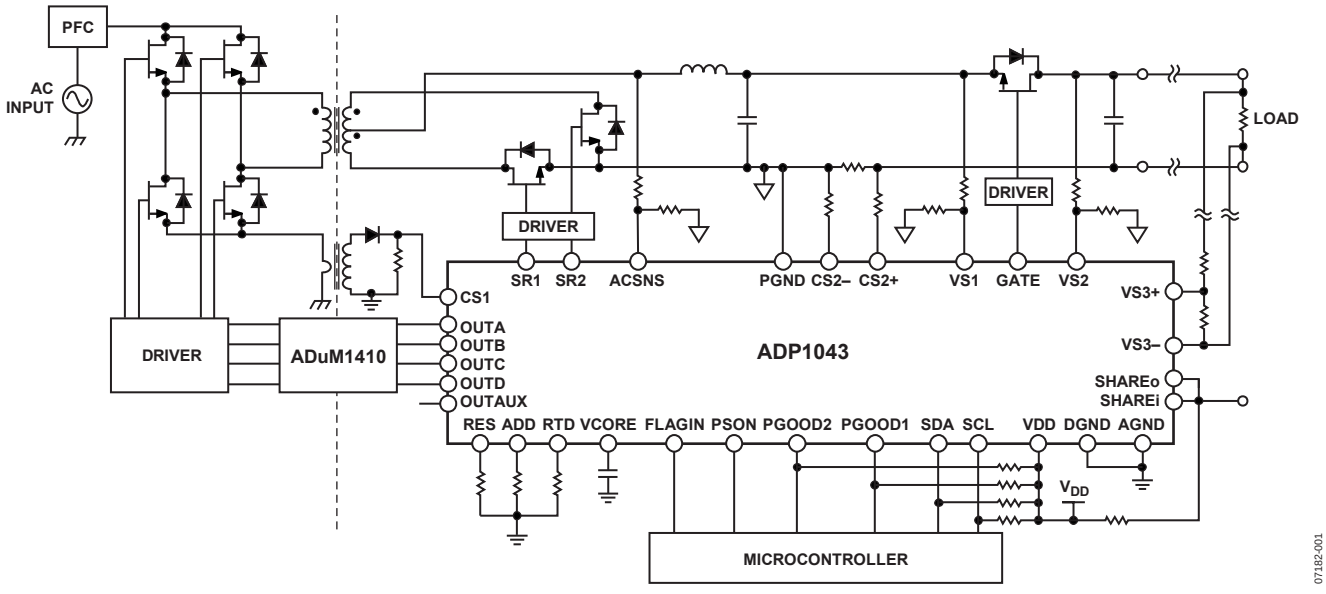

Figure 1.

Rev. 0

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REVISION HISTORY

4/09—Revision 0: Initial Version

The ADP1043 is a secondary side controller for switch mode power supplies (SMPS). It is designed for use in isolated redundant applications. The ADP1043 integrates the typical functions that are needed to control a power supply. These include

- Output voltage sense and feedback
- Digital loop filter compensation
- PWM generation
- Current sharing
- Current, voltage, and temperature sense
- Housekeeping and I²C interface
- Calibration and trimming

The main function of controlling the output voltage is performed using the feedback ADCs, the digital loop filter, and the PWM block. The feedback ADCs use a multipath approach (patent pending). The ADP1043 combines a high speed, low resolution (fast and coarse) ADC and a low speed, high resolution (slow and accurate) ADC. Loop compensation is implemented using the digital filter. This PID (proportional, integral, derivative) filter is implemented in the digital domain to allow easy programming of filter characteristics, which is of great value in customizing and debugging designs.

The PWM block generates up to seven programmable PWM outputs for control of FET drivers and synchronous rectification FET drivers. This programmability allows many traditional and unique switching topologies to be realized. A current share bus interface is provided for parallel power supplies.

Conventional power supply housekeeping features, such as remote and local voltage sense and primary and secondary side current sense, are included. An extensive set of protections is offered, including overvoltage protection (OVP), overcurrent protection (OCP), overtemperature protection (OTP), undervoltage protection (UVP), ground continuity monitoring, and ac sensing.

All these features are programmable through the I²C bus interface. Other information, such as input current, output current, and fault flags, is also available through the I²C bus interface.

The internal EEPROM can store all programmed values and allows standalone control without a microcontroller. A free, downloadable GUI is available that provides all the necessary software to program the ADP1043. For more information about the GUI, contact Analog Devices, Inc., for the latest software and a user's guide.

The ADP1043 operates from a single 3.3 V supply and is specified from −40°C to +85°C.

FUNCTIONAL BLOCK DIAGRAM

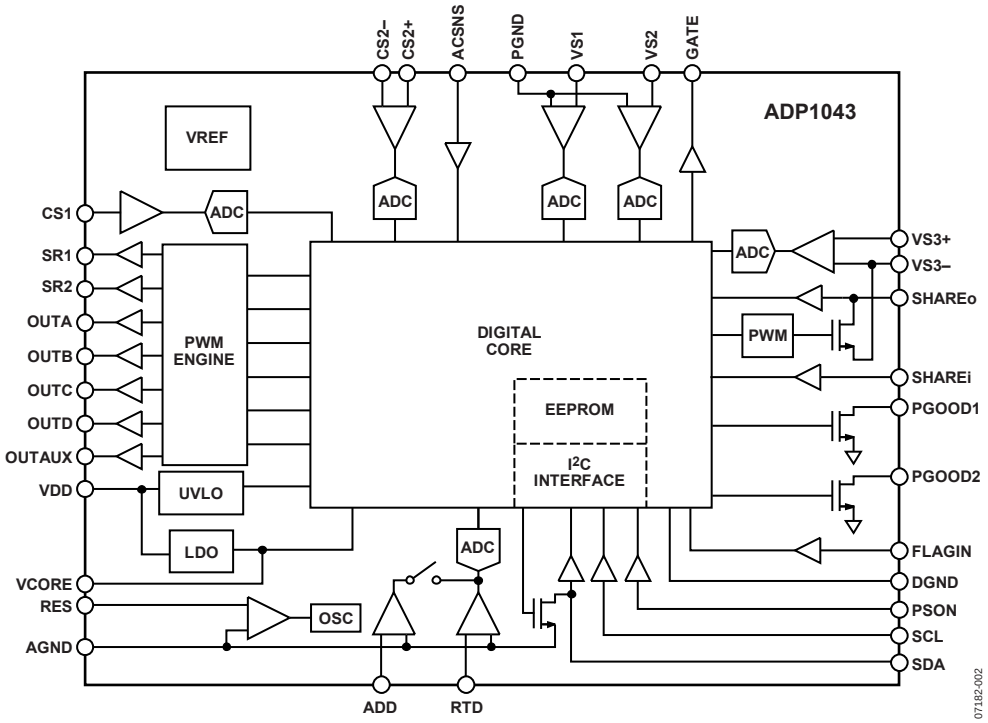

Figure 2.

SPECIFICATIONS

V_{DD} = 3.3 V, T_A = −40°C to +85°C, unless otherwise noted. FSR = full-scale range.

Table 1.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SUPPLY						
V_{DD}	V_{DD}		3.23	3.3	3.6	V
I_{DD}	I_{DD}	Normal operation (PSON is high)		20		mA
		Power supply off (PSON is low)		15		mA
		During EEPROM programming (40 ms)		I_{DD} + 8		mA
POWER-ON RESET						
Power-On Reset		V_{DD} rising	3.19			V
UVLO		V_{DD} falling	2.75	2.85	2.95	V
UVLO Hysteresis				35		mV
VCORE PIN						
Output Voltage		T_A = 25°C	2.3	2.5	2.7	V
OSCILLATOR AND PLL						
PLL Frequency		RES = 49.9 kΩ	190	200	210	MHz
OUTA, OUTB, OUTC, OUTD, OUTAUX, SR1, SR2 PINS						
Output Low Voltage	V_{OL}	Source current = 10 mA			0.4	V
Output High Voltage	V_{OH}	Source current = 10 mA	V_{DD} − 0.4			V
Rise Time		C_{LOAD} = 50 pF		3.5		ns
Fall Time		C_{LOAD} = 50 pF		1.5		ns
VS1, VS2, VS3 LOW SPEED ADC						
Input Voltage Range	V_{IN}	Differential voltage from VS1, VS2 to PGND, and VS3+ to VS3−	0	1	1.58	V
Sampling Frequency	f_{SAMP}			100		Hz
Voltage Sense Measurement Accuracy		From 10% to 90% of input voltage range	−3.5		+3.5	% FSR
			−55		+55	mV
		From 0% to 100% of input voltage range	−10		+10	% FSR
			−158		+158	mV
		From 900 mV to 1.1 V	−2.5		+2.5	% FSR
			−39.5		+39.5	mV
Voltage Sense Measurement Resolution				12		Bits
Voltage Differential from VS3− to PGND			−200		+200	mV
VS1 OVP Comparator Speed				650		µs
VS1 OVP Threshold Accuracy		Relative to nominal voltage (1 V) on VS1		2.5		%
VS1 HIGH SPEED ADC						
Sampling Frequency	f_{SAMP}			800		kHz
Resolution				5		Bits
Dynamic Range				±18		mV
CURRENT SENSE 1 (CS1 PIN)						
Input Voltage Range	V_{IN}		0	1	1.58	V
Sampling Frequency	f_{SAMP}			100		Hz
Current Sense Measurement Accuracy		From 10% to 90% of input voltage range	−3.5		+3.5	% FSR
			−55		+55	mV
		From 0% to 100% of input voltage range	−10		+10	% FSR
			−158		+158	mV

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
Current Sense Measurement Resolution				12		Bits
CS1 Fast OCP Threshold			1.14	1.2	1.26	V
CS1 Fast OCP Speed		Time to shut down PWM		80	100	ns
CS1 Accurate OCP Accuracy		From 10% to 90% of input voltage range	−3.5		+3.5	% FSR
			−55		+55	mV
CS1 Accurate OCP Speed				10		ms
CURRENT SENSE 2 (CS2+, CS2− PINS)						
ADC Input Voltage Range		LSB = 61.035 µV	0		225	mV
Sampling Frequency	f_{SAMP}			100		Hz
Current Sense Measurement Accuracy		From 0 mV to 200 mV	−5		+5	mV
		From 200 mV to 225 mV	−20		+20	mV
			−10		+10	% FSR
Current Sense Measurement Resolution				12		Bits
CS2 Accurate OCP Accuracy		From 0 mV to 200 mV (Register 0x23[7:6] = 10)	−5		+5	mV
			−2.5		+2.5	% FSR
CS2 Accurate OCP Speed				10		ms
Current Source (Low Side)		Resistor tolerance must be <0.1%		100		µA
Common-Mode Voltage at the CS2+ and CS2− Pins		To achieve CS2 measurement accuracy	0.8	1	1.3	V
GATE PIN (OPEN DRAIN)						
Output Low Voltage	V_{OL}				0.4	V
RTD PIN						
Current Source		RTD resistor = 100 kΩ	9.0	10	12	µA
RTD ADC Measurement Accuracy[1]		From 2% to 20% of input voltage range	−1		+1	% FSR
		From 32 mV to 320 mV (not factory calibrated)	−15.8		+15.8	mV
		From 0% to 100% of input voltage range	−10		+10	% FSR
		From 0 V to 1.58 V	−158		+158	mV
OTP Threshold Accuracy		When RTD = 10 kΩ	−0.5		+0.5	% FSR
			−7.9		+7.9	mV
		When RTD = 100 kΩ	−10		+10	% FSR
			−158		+158	mV
OTP Speed				10		ms
OTP Threshold Hysteresis		When RTD = 10 kΩ		16		mV
PGOOD1, PGOOD2, SHAREo PINS (OPEN DRAIN)						
Output Low Voltage	V_{OL}				0.4	V
PSON, FLAGIN, SHAREi PINS (DIGITAL INPUTS)						
Input Low Voltage	V_{IL}				0.4	V
Input High Voltage	V_{IH}		V_{DD} − 0.8			V
SDA/SCL PINS		V_{DD} = 3.3 V				
Input Low Voltage	V_{IL}				0.4	V
Input High Voltage	V_{IH}		V_{DD} − 0.8			V
Output Low Voltage	V_{OL}				0.4	V
Leakage Current		Tristate	−5		+5	µA

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
SERIAL BUS TIMING						
Clock Frequency				100	400	kHz
Glitch Immunity	t_{SW}				50	ns
Bus Free Time	t_{BUF}		4.7			µs
Start Setup Time	$t_{SU;STA}$		4.7			µs
Start Hold Time	$t_{HD;STA}$		4			µs
SCL Low Time	t_{LOW}		4.7			µs
SCL High Time	t_{HIGH}		4			µs
SCL, SDA Rise Time	t_R				1000	ns
SCL, SDA Fall Time	t_F				300	ns
Data Setup Time	$t_{SU;DAT}$		250			ns
Data Hold Time	$t_{HD;DAT}$		300			ns
EEPROM RELIABILITY						
Endurance[2]			10,000			Cycles
Data Retention[3]		T_J = 85°C	20			Years

[1] The RTD ADC does not meet this specification when shipped from the factory. It must be recalibrated to achieve this specification. The part is factory calibrated for OTP accuracy rather than temperature measurement.
[2] Endurance is qualified as per JEDEC Standard 22 Method A117 and measured at −40°C, +25°C, +85°C, and +125°C.
[3] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22 Method A117. Retention lifetime derates with junction temperature.

ABSOLUTE MAXIMUM RATINGS

Table 2.

Parameter	Rating
Supply Voltage (Continuous) VDD	3.8 V
Digital Pins	−0.3 V to V_{DD} + 0.3 V
VS3− to PGND, AGND, DGND	−0.3 V to +0.3 V
RTD, VS1 to AGND	2.5 V
Operating Temperature Range	−40°C to +85°C
Storage Temperature Range	−65°C to +150°C
Junction Temperature	150°C
Peak Solder Reflow Temperature	
SnPb Assemblies (10 sec to 30 sec)	240°C
RoHS-Compliant Assemblies (20 sec to 40 sec)	260°C
ESD Charged Device Model	1.5 kV
ESD Human Body Model	1.5 kV

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages.

Table 3. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
32-Lead LFCSP	44.4	6.4	°C/W

SOLDERING

It is important to follow the correct guidelines when laying out the PCB footprint for the ADP1043 and for soldering the part onto the PCB. The AN-772 Application Note discusses this topic in detail (see www.analog.com).

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

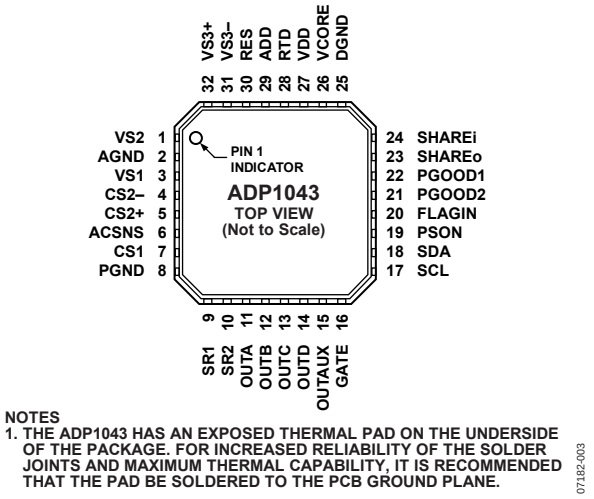

Figure 3. Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	VS2	Power Supply Output Sense Input. This signal is referred to PGND. Input to a low frequency Σ-Δ ADC. Nominal voltage at this pin should be 1 V.
2	AGND	Analog Ground. This pin is the ground for the analog circuitry of the ADP1043. Star connect to DGND.
3	VS1	Local Voltage Sense Input. This signal is referred to PGND. Input to a high frequency Σ-Δ ADC. Nominal voltage at this pin should be 1 V.
4	CS2–	Inverting Differential Current Sense Input. Nominal voltage at this pin should be 1 V for best operation. Place a 10 kΩ resistor between the sense resistor and this pin. The tolerance on the resistor must be better than 0.1%.
5	CS2+	Noninverting Differential Current Sense Input. Nominal voltage at this pin should be 1 V for best operation. Place a 10 kΩ resistor between the sense resistor and this pin. The tolerance on the resistor must be better than 0.1%.
6	ACSNS	AC Sense Input. This input is connected upstream of the main inductor through a resistor divider network. The nominal voltage at this pin should be 1 V. This signal is referred to PGND.
7	CS1	Primary Side Current Sense Input. This pin is the current transformer input to measure and control the primary side current. This signal is referred to PGND.
8	PGND	Power Ground. This pin is the ground connection for the main power rail of the power supply. Star connect to AGND.
9	SR1	Synchronous Rectifier Output. This PWM output is connected to the input of a FET driver. This pin can be disabled when not in use. This signal is referred to AGND.
10	SR2	Synchronous Rectifier Output. This PWM output is connected to the input of a FET driver. This pin can be disabled when not in use. This signal is referred to AGND.
11	OUTA	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referred to AGND.
12	OUTB	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referred to AGND.
13	OUTC	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referred to AGND.
14	OUTD	PWM Output for Primary Side Switch. This pin can be disabled when not in use. This signal is referred to AGND.
15	OUTAUX	Auxiliary PWM Output. This pin can be disabled when not in use. This signal is referred to AGND.
16	GATE	Gate Drive Output (Open Drain). This signal is referred to AGND.
17	SCL	I^2C Serial Clock Input. This signal is referred to AGND.
18	SDA	I^2C Serial Data Input and Output (Open Drain). This signal is referred to AGND.
19	PSON	Power Supply On Input. This signal is referred to DGND.
20	FLAGIN	Flag Input. An external signal can be input at this pin to generate a flag condition.

Pin No.	Mnemonic	Description
21	PGOOD2	Power-Good Output (Open Drain). This signal is referred to AGND. This pin is controlled by the PGOOD2 flag. This pin is set if any flag is set.
22	PGOOD1	Power-Good Output (Open Drain). This signal is referred to AGND. This pin is controlled by the PGOOD1 flag. This pin is set if any of the following are out of range: CS1 OCP, CS2 OCP, VS1 OVP, or UVP.
23	SHAREo	Share Bus Output Voltage Pin. Connect this pin to 3.3 V through a 2.2 kΩ resistor. When configured as a digital share bus, this pin is a digital output. This signal is referred to AGND.
24	SHAREi	Share Bus Feedback Pin. Connect this pin to the SHAREo pin. This signal is input to an ADC in the ADP1043. This signal is referred to AGND.
25	DGND	Digital Ground. This pin is the ground for the digital circuitry of the ADP1043. Star connect to AGND.
26	VCORE	Output of 2.5 V Regulator. Connect a 100 nF capacitor from this pin to DGND.
27	VDD	Positive Supply Input. Range is from 3.23 V to 3.6 V. This signal is referred to AGND.
28	RTD	Thermistor Input. A 100 kΩ thermistor is placed from this pin to AGND. This signal is referred to AGND.
29	ADD	Address Select Input. Connect a resistor from ADD to AGND. This signal is referred to AGND.
30	RES	Resistor Input. This pin sets up the internal voltage reference for the ADP1043. Connect a 49.9 kΩ resistor (±0.1%) from RES to AGND. This signal is referred to AGND.
31	VS3−	Inverting Remote Voltage Sense Input. There should be a low ohmic connection to AGND.
32	VS3+	Noninverting Remote Voltage Sense Input. This signal is referred to VS3−.
Exposed Pad	EP	The ADP1043 has an exposed thermal pad on the underside of the package. For increased reliability of the solder joints and maximum thermal capability, it is recommended that the pad be soldered to the PCB ground plane.

THEORY OF OPERATION

CURRENT SENSE

The ADP1043 has two individual current sense inputs: CS1 and CS2±. These inputs sense, protect, and control the output current and the share bus information. They are factory calibrated.

CS1 Operation (CS1)

CS1 is typically used for the monitoring and protection of the primary side current. This is commonly known as the current transformer (CT) method of current sensing. The input signal at the CS1 pin is fed into an ADC for current monitoring. The range of the ADC is 0 V to 1.58 V. The input signal is also fed into a comparator for fast OCP protection. The typical configuration for the current sense is shown in Figure 4.

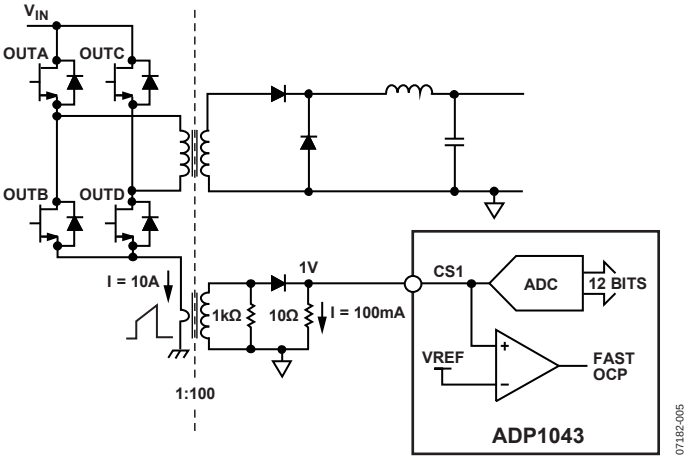

Figure 4. Current Sense 1 (CS1) Operation

The comparator measures peak current, and the ADC measures the average current information. This information is available through the I²C interface. Various thresholds and limits can be set for CS1, such as OCP. These thresholds and limits are described in the Current Sense and Current Limit Registers section.

CS2 Operation (CS2+, CS2–)

CS2± is typically used for the monitoring and protection of the secondary side current. The full-scale range of the CS2 ADC is 225 mV. The nominal full load voltage drop can be configured for 37.5 mV, 75 mV, or 150 mV using a sense resistor. The inputs are differential and are fed into an ADC through a pair of external resistors. When using low-side current sense, a 10 kΩ resistor is required. A typical configuration is shown in Figure 5. Various thresholds and limits can be set for CS2, such as OCP. These thresholds and limits are described in the Current Sense and Current Limit Registers section.

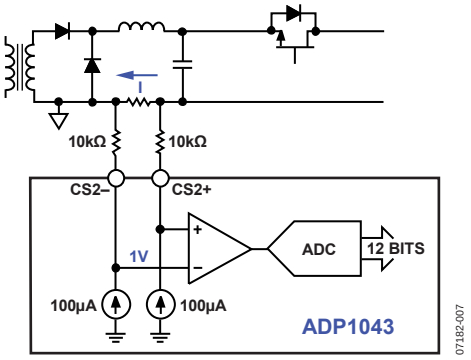

Figure 5. Low-Side Resistive Current Sense

VOLTAGE SENSE AND CONTROL LOOP

Multiple voltage sense inputs on the ADP1043 are used for the monitoring, control, and protection of the power supply output. The voltage information is available through the I²C interface. All voltage sense points are factory calibrated and stored in the EEPROM of the ADP1043.

The update rate of the ADC from a control loop standpoint is set to the switching frequency. Therefore, if the switching frequency is set to 100 kHz, the ADC outputs a signal every 100 kHz to the control loop. Because the ADCs sample at 1.6 MHz, the output of the ADC is the average of the 16 readings that it takes during that 100 kHz time frame.

From a voltage monitoring standpoint, the VS1, VS2, and VS3 voltage value registers are updated every 10 ms. The ADP1043 stores every ADC sample for 10 ms and then outputs the average value at the end of the 10 ms period. Therefore, if these registers are read at least every 10 ms, a true average value is read. The same applies to the CS1 and CS2 current readings.

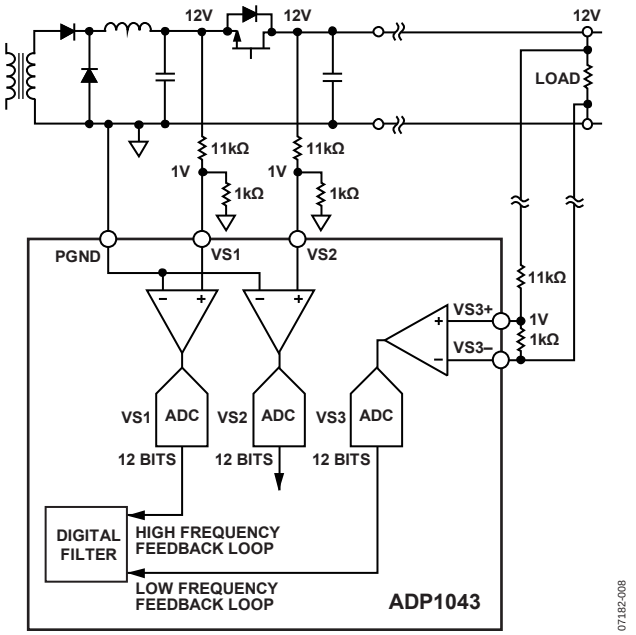

Figure 6. Voltage Sense Configuration

VS1 Operation (VS1)

VS1 is used for the monitoring and protection of the power supply voltage at the output of the LC stage. This is also the high frequency feedback loop for the power supply. The VS1 sense point on the power rail needs an external resistor divider to bring the nominal common-mode signal to 1 V at the VS1 pin (see Figure 6). The resistor divider is necessary because the ADP1043 VS1 ADC input range is 0 V to 1.58 V. This divided-down signal is internally fed into a high speed Σ-Δ (sigma-delta) ADC. The output of the VS1 ADC goes to the digital filter.

The ADC has a bandwidth of 2 MHz and is run from a 25 MHz clock. It has a range of ±18 mV. When the sampling rate is 200 kHz, there is 0.6 mV (2 LSBs) of quantization noise. Increasing the sampling rate to 400 kHz increases the quantization noise to 1.2 mV.

In the event of a load overvoltage condition, the power supply is regulated from the VS1 sense point, rather than from the VS3 point.

VS2 Operation (VS2)

VS2 is typically used for the monitoring and protection of the output of the power supply. The VS2 sense point on the power rail needs an external resistor divider to bring the nominal common-mode signal to 1 V at the VS2 pin (see Figure 6). The resistor divider is necessary because the ADP1043 VS2 ADC input range is 0 V to 1.58 V. This divided-down signal is internally fed into an ADC. The output of the VS2 ADC goes to the VS2 voltage value register (Register 0x16).

VS3 Operation (VS3+, VS3–)

VS3± is used for the monitoring and protection of the remote load voltage. It is a fully differential input. This is the main feedback sense point for the power supply control loop. The VS3 sense point on the power rail needs an external resistor divider to bring the nominal common-mode signal to 1 V at the VS3± pins (see Figure 6). The resistor divider is necessary because the ADP1043 VS3 ADC input range is 0 V to 1.58 V. This divided-down signal is internally fed into an ADC. The output of the VS3 ADC goes to the digital filter.

ADCs

The ADP1043 includes several ADCs. The high speed ADC is described in the VS1 Operation (VS1) section. The other ADCs are low speed, high resolution. They have a 1 kHz bandwidth and 12-bit resolution. Each ADC has its own voltage reference for added protection from potential failure. The digital output of each ADC is readable through the value registers.

DIGITAL FILTER

The loop response of the power supply can be changed using the internal programmable digital filter. A Type 3 filter architecture has been implemented. To tailor the loop response to the specific application, the low frequency gain, zero location, pole location, and high frequency gain can all be set individually. It is recommended that the Analog Devices software GUI be used to program the filter. The software GUI displays the filter response in Bode plot format and can be used to calculate all stability criteria for the power supply.

The digital filter introduces an extra phase delay element into the control loop. The digital filter circuit sends the duty cycle information to the PWM circuit at the beginning of each switching cycle (unlike an analog controller, which makes the decision on the duty cycle information constantly). This approach has no phase delay associated with it. Therefore, the extra phase delay, Φ, introduced by the filter block is

$$\Phi = 180 \times (f/f_{SW})$$

where f_{SW} is the switching frequency.

At one tenth of the switching frequency, the phase delay is 18°. The GUI incorporates this phase delay into its calculations.

PWM AND SYNC RECT OUTPUTS (OUTA, OUTB, OUTC, OUTD, OUTAUX, SR1, SR2)

The PWM and SR outputs are used for control of the primary side drivers and the synchronous rectifier drivers. They can be used for several control topologies, including full-bridge, phase shift ZVS, and interleaved two switch forward converter configurations. Delays between rising and falling edges can be individually programmed. Special care must be taken to avoid shoot-through and cross-conduction. It is recommended that the Analog Devices software GUI be used to program these outputs. Figure 7 shows an example configuration to drive a full-bridge, phase shift topology with synchronous rectification.

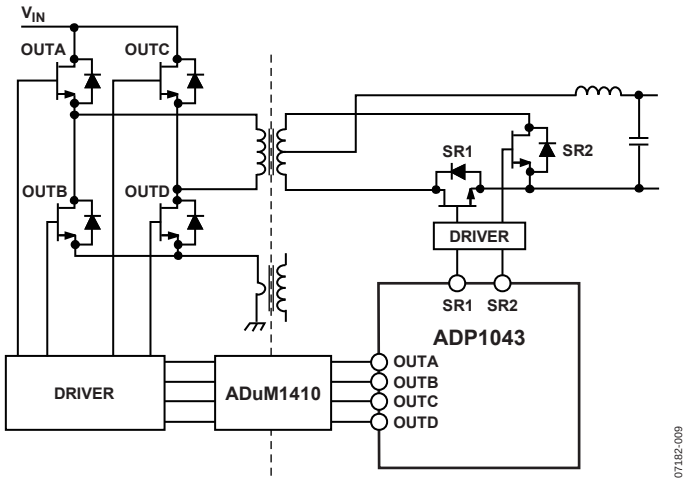

Figure 7. PWM Pin Assignment

The PWM and SR outputs all work together. Therefore, when reprogramming more than one of these outputs, it is important to first update all the registers, then latch the information into the ADP1043 at one time. During reprogramming, the outputs are temporarily disabled. A special instruction is sent to the ADP1043 to ensure that new timing information is programmed simultaneously. It is recommended that any PWM outputs be disabled when not in use.

OUTAUX is an additional PWM output pin; OUTAUX allows an extra PWM signal to be generated at a different frequency from the other six PWM outputs. This signal can be used to drive an extra power converter stage, such as a buck controller located in front of a full-bridge converter. OUTAUX can also be used as a clock reference signal.

Note that if a PWM modulating edge tries to go to a value less than 0, it can cause the PWM to output a constant high signal. This condition must be avoided to prevent damage to the power supply.

MODULATION LIMIT

Using the modulation limit register (Register 0x2E), it is possible to apply a maximum modulation limit and a minimum modulation limit to any PWM signal, thus limiting the modulation range of any PWM. These limits are a percentage of the switching period. If the modulation required is lower than the minimum setting, pulse skipping can be enabled.

Following is an example of how to use the modulation limit settings. In this example, the switching cycle period is 4 µs and modulation on the t2 edge (falling edge) is enabled. The nominal position of t2 is set to 1.6 µs, which is 40% of the 4 µs period. The modulation high limit is set to (nominal + 50%). Therefore, the modulation high limit is (40% + 50%) = 90% of the switching cycle period; 90% of 4 µs = 3.6 µs. The modulation low limit is set to (nominal − 35%). Therefore, the modulation low limit is (40% − 35%) = 5% of the switching cycle period; 5% of 4 µs = 0.2 µs.

Figure 8. Setting Modulation Limits

The GUI provided with the ADP1043 is recommended for evaluating this feature of the ADP1043.

POWER GOOD/SOFT START

The ADP1043 has two power-good pins. The PGOOD1 pin and fault flag are set when any of the following conditions are out of range: CS1 OCP, CS2 OCP, VS1 OVP, or UVP. The PGOOD2 pin and fault flag are set when any flag is set. The PGOOD2 pin can also be used as an interrupt pin to notify a host controller that a flag has been set. The polarity of both pins can be configured as active high or active low.

If a CS1 fast OCP fault condition occurs during soft start, the entire soft start routine is reset, and the ADP1043 begins another soft start routine. All other fault flags are ignored during soft start.

A dedicated filter is used during soft start. The filter is disabled at the end of the soft start routine, and the voltage loop digital filter is used.

Soft Start

When the user turns on the power supply (enables PSON), the following soft start procedure occurs:

1. The PSON signal is enabled at Time t0. The ADP1043 checks that initial flags are OK. These flags include VDD OK and GND OK.
2. The ADP1043 waits for Time t_1 before it begins soft start. The length of t_1 is set in Register 0x2D, Bits[7:6].
3. The soft start begins to ramp up the power supply voltage at the start of Time t_2.
4. The ADP1043 keeps the GATE signal turned off. The voltage differential increases (VS1 − VS2). When the voltage differential reaches approximately 120 mV, the gate signal is enabled at Time t_3. The ADP1043 begins to regulate voltage from VS3 instead of VS1.
5. After the power supply voltage increases above the VS1 UVP undervoltage limit (Register 0x34, Bits[3:0]), at the end of Time t4, the UVP flag is reset.
6. After the UVP flag is reset and provided that all other PGOOD1 fault conditions are OK, the PGOOD1 signal waits for Time t_5 before it is enabled. The length of t_5 is programmable in Register 0x2C, Bits[7:6].

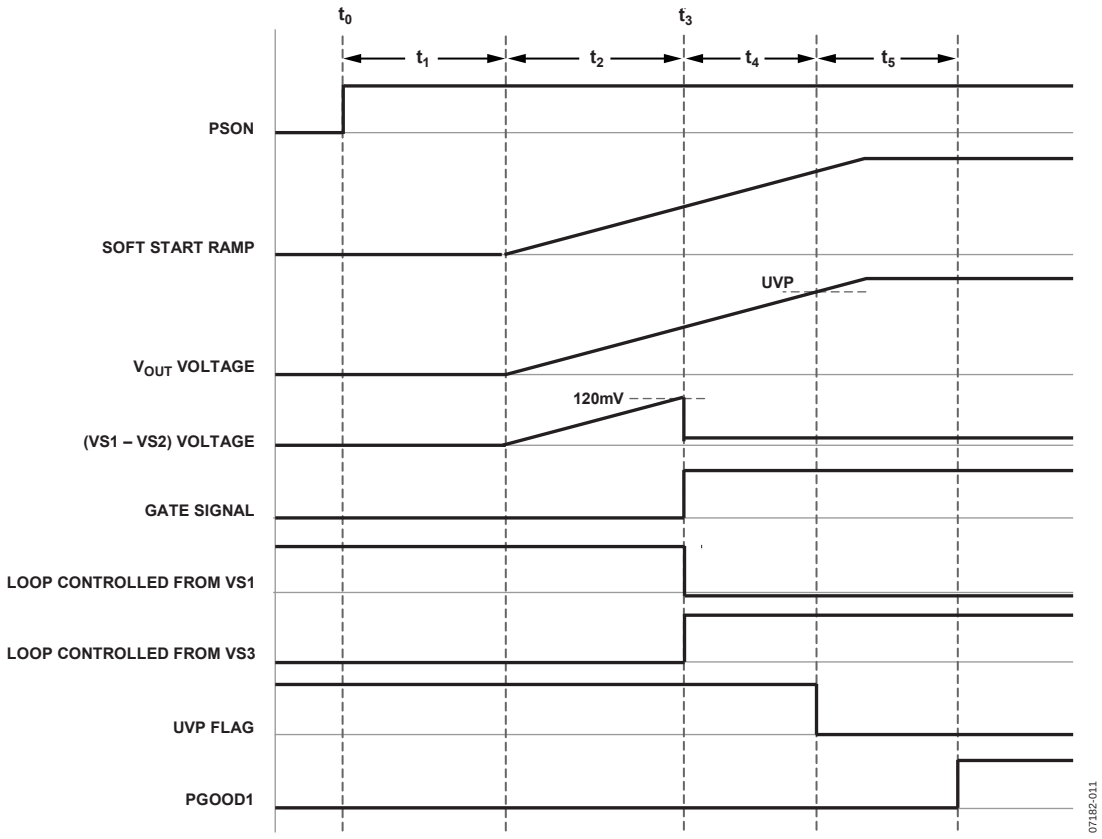

Figure 9. Soft Start Timing Diagram

DIGITAL SHARE BUS (SHARE)

Using Register 0x2A, Bit 6, it is possible to program the ADP1043 to use the CS1 current information or the CS2 current information for current sharing.

The digital share bus is based on a single-wire communication bus principle. This means that the clock and data signals are contained together.

The ADP1043 outputs a digital word onto the share bus. The digital word is a function of the current that the power supply is providing (the higher the current, the larger the digital word). The power supply with the highest current controls the bus (master). A power supply that is putting out less current (slave) sees that another supply is providing more power to the load than it is. During the next cycle, the slave increases its current output contribution by increasing its output voltage. This cycle continues until the slave outputs the same current as the master, within a programmable tolerance range. Figure 10 shows the configuration of the digital share bus.

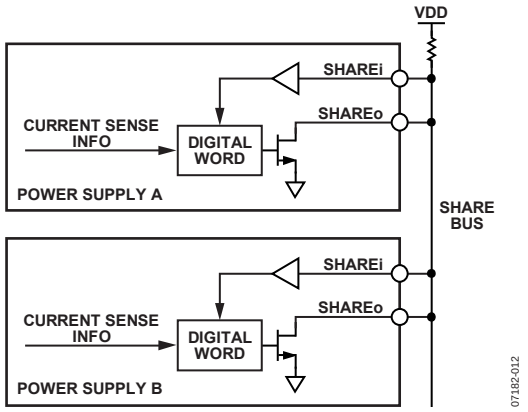

Figure 10. Digital Share Bus Configuration

When two or more ADP1043s are connected, they synchronize their share bus timing. This synchronization is performed by the start bit at the beginning of a communications frame. If a new ADP1043 is hot-swapped onto an existing digital share bus, it waits to begin sharing until the next frame. The new ADP1043 monitors the share bus until it sees a stop bit, which designates the end of a share frame. It then performs synchronization with the other ADP1043s during the next start bit. The digital share bus frame is shown in Figure 12.

Figure 11 shows the possible signals on the share bus.

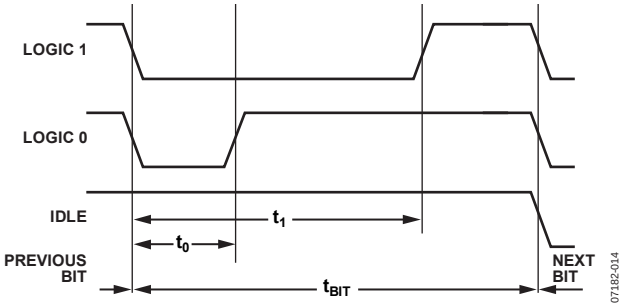

Figure 11. Share Bus High, Low, and Idle Bits

The length of a bit (t_{BIT}) is fixed at 10 µs. A Logic 1 is defined as a high-to-low transition at the start of the bit and a low-to-high transition at 75% of t_{BIT}. A Logic 0 is defined as a high-to-low transition at the start of the bit and a low-to-high transition at 25% of t_{BIT}.

The bus is idle when the bus is high during the whole period of t_{BIT}. All other activity on the bus is illegal. Glitches up to t_{GLITCH} (200 ns) are ignored.

It is recommended that a 200 Ω resistor be placed between the SHAREi pin and the share bus to improve sharing performance.

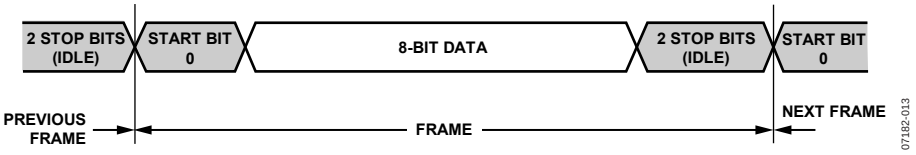

Figure 12. Digital Share Bus Frame Timing Diagram

POWER SUPPLY SYSTEM AND FAULT MONITORING

The ADP1043 has extensive system and fault monitoring capabilities. The system monitoring functions include voltage, current, power, and temperature readings. The fault conditions include out-of-limit values for current, voltage, power, and temperature. The limits for the fault conditions are programmable. The ADP1043 has an extensive set of flags that are set when certain thresholds or limits are reached. These thresholds and limits are explained in the Fault Registers section.

FLAGS

The ADP1043 has an extensive set of flags that are set when certain limits, conditions, and thresholds are reached. The status of these flags can be read in Register 0x00 to Register 0x03. The response to these flags is individually programmable. Flags can be ignored or used to perform tasks such as turning off certain PWMs or the GATE signal. Flags can also be used to turn off the power supply. The ADP1043 can also be programmed to respond when these flags are reset. For more information, see Register 0x08 to Register 0x0E.

The ADP1043 also has a set of latched fault registers (Register 0x04 to Register 0x07). The latched fault registers have the same flags as Register 0x00 to Register 0x03, but the flags in the latched registers remain set so that an intermittent fault can be detected. Reading a latched register resets all the flags in that register.

MONITORING FUNCTIONS

The ADP1043 monitors and reports several signals, including voltages, currents, power, and temperature. All these values are stored in individual registers and can be read through the I²C interface. See the Value Registers section for more details.

VOLTAGE READINGS

When there is exactly 1 V on the VS1 and VS2 pins, the equivalent register readings report 2592 (0xA20). In a 12 V application, the 12 V reading is divided down using a resistor divider network to provide 1 V at the sense pin. Therefore, to convert the register value to a real voltage, use the following formula:

$$V_{OUT} = (VS1\_Voltage\_Value/2592) \times ((R1 + R2)/R2)$$

where *R1* and *R2* are the external resistor divider values between the power supply output and the VS1 pin.

In a 12 V system, this equates to

$$V_{OUT} = (VS1\_Voltage\_Value/2592) \times ((11\ k\Omega + 1\ k\Omega)/1\ k\Omega)$$

For example, if VS1_Voltage_Value = 2592, the real voltage is calculated as follows:

$$V_{OUT} = (2592/2592) \times 12\ V$$

$$V_{OUT} = 12\ V$$

CURRENT READINGS

CS1 Pin

When there is exactly 1 V on the CS1 pin, the value in the CS1 value register (Register 0x13) reads 2592 (0xA20).

CS2 Pin

The user sets the full-scale (FS) voltage drop (37.5 mV, 75 mV, or 150 mV) that is present across the R_{SENSE} sense resistor (by programming Register 0x23, Bits[7:6]). When this full-scale voltage is present across R_{SENSE}, the CS2 value register (Register 0x18) outputs 2458 (0x99A).

Therefore, to convert the CS2 value reading to a real current, use the following formula:

$$I_{OUT} = (CS2\_Value/2458) \times (FS/R_{SENSE})$$

where:
FS is the full-scale voltage drop.
R_{SENSE} is the sense resistor value.

For example, if CS2_Value = 2300, R_{SENSE} = 20 mΩ, and FS = 150 mV, the real current is calculated as follows:

$$I_{OUT} = (2300/2458) \times (150\ mV/20\ m\Omega)$$

$$I_{OUT} = 7.02\ A$$

POWER READINGS

The output power value register (Register 0x19) is the product of the VS3 voltage value and the CS2 current value. This register is a 16-bit word. It multiplies two 12-bit numbers and discards the eight LSBs.

$$P_{OUT} = (V_{OUT}) \times (I_{OUT})$$

$$P_{OUT} = ((VS3\_Voltage\_Value/2592) \times ((R1 + R2)/R2)) \times ((CS2\_Value/2458) \times (FS/R_{SENSE}))$$

From the example given in the previous section

$$P_{OUT} = (12\ V) \times (7.02\ A) = 84.24\ W$$

FIRST ERROR FAULT ID AND VALUE REGISTERS

When the ADP1043 registers several fault conditions, it stores the value of the first fault in a dedicated register. For example, if the overtemperature (OTP) fault is registered, followed by another fault, the temperature flag and the value when the fault occurred is stored in the first flag ID register (Register 0x10) and the first flag value register (Register 0x11). These registers give the user more information for fault diagnosis than a simple flag. The contents of these registers are latched, meaning that they are stored until read by the user.

EXTERNAL FLAG INPUT (FLAGIN)

The FLAGIN pin can be used to send an external fault signal into the ADP1043. The reaction to this flag can be programmed in the same way as the internal flags.

TEMPERATURE READINGS (RTD PIN)

The RTD pin is set up for use with an external 100 kΩ NTC thermistor. The RTD pin has an internal 10 µA current source. Therefore, with a 100 kΩ thermistor, the voltage on the RTD pin is 1 V at 25°C. An ADC on the ADP1043 monitors the voltage on the RTD pin.

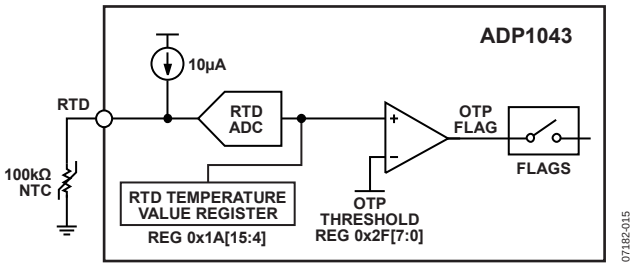

Figure 13. RTD Pin Internal Details

The output of the RTD ADC is linearly proportional to the voltage on the RTD pin. However, thermistors exhibit a nonlinear function of resistance vs. temperature. Therefore, it is necessary to perform some postprocessing on the RTD ADC reading to accurately read the temperature. This postprocessing can be in the form of a lookup table or polynomial equation to match the specific NTC being used.

POWER MONITORING ACCURACY

The ADP1043 power monitoring accuracy is specified relative to the full-scale range of the signal that it is measuring.

OVERTEMPERATURE PROTECTION (OTP)

If the temperature being sensed at the RTD pin exceeds the programmable threshold, the OTP flag is set. There are 16 mV of hysteresis on this flag (see Register 0x2F for details). The response to the OTP flag is programmable.

The RTD trim is performed to be accurate at the lower end of the RTD ADC. This gives a more accurate measurement for determining the OTP threshold.

OVERCURRENT PROTECTION (OCP)

The ADP1043 has several OCP functions. CS1 and CS2 have individual OCP circuits to provide both primary and secondary side protection.

CS1 has two protection circuits: CS1 fast OCP and CS1 accurate OCP (see Figure 14). CS1 fast OCP is an analog comparator. When the voltage at the CS1 pin exceeds the (fixed) 1.2 V threshold, the CS1 fast OCP flag is set. A blanking time can be set to ignore the current spike at the beginning of the current signal. A debounce can also be programmed to improve the noise immunity of the OCP circuit. When the CS1 fast OCP is set, all PWMs are immediately disabled for the remainder of the switching cycle. They are reenabled at the start of the next switching cycle. This function can be disabled if not needed.

CS1 accurate OCP is used for more precise control of overcurrent protection. With CS1 accurate OCP, the reading at the output of the CS1 ADC (Register 0x13) is compared to a programmable OCP value. The CS1 OCP value can be programmed from 0 to 254 decimal using Register 0x22. If the CS1 reading exceeds the CS1 OCP value, the CS1 accurate OCP flag is set. The speed of this decision is 10 ms. The response to the flag is programmable.

CS2 has one protection circuit, called CS2 accurate OCP. The reading at the output of the CS2 ADC (Register 0x18) is compared to a programmable OCP threshold. The CS2 OCP threshold can be programmed from 0 to 2976 decimal using Register 0x26, Bits[4:0]. If the CS2 reading exceeds the CS2 OCP threshold, the CS2 accurate OCP flag is set. The speed of this decision is 10 ms. The response to the flag is programmable.

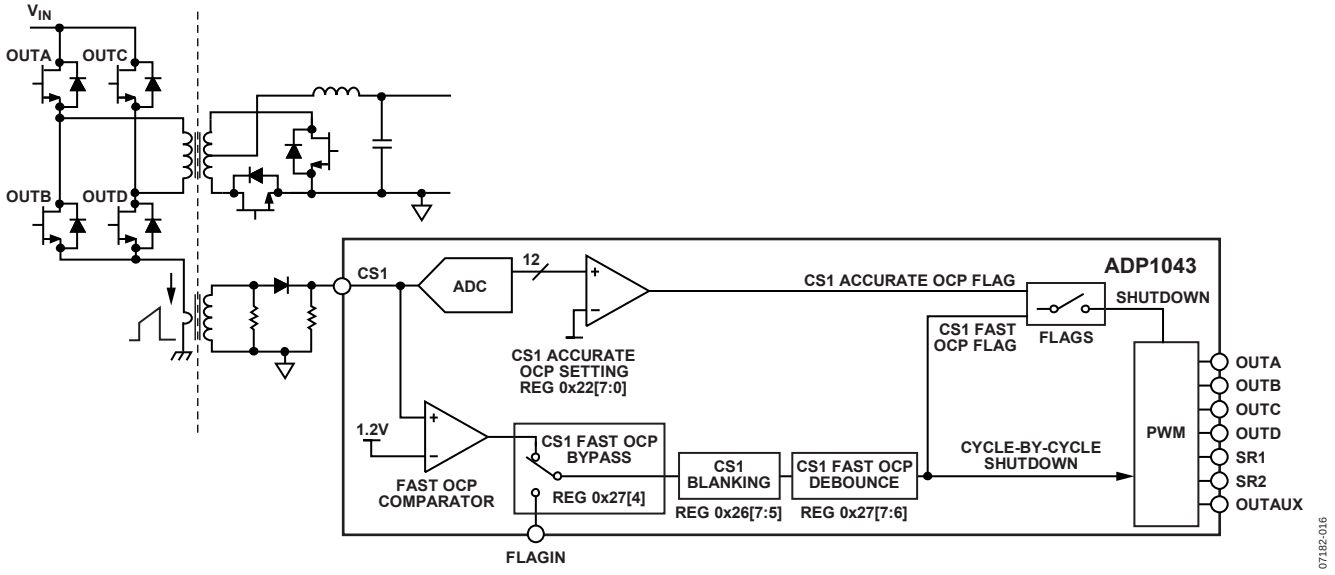

Figure 14. CS1 OCP Detailed Internal Schematic

OVERVOLTAGE PROTECTION (OVP)

The ADP1043 has one OVP circuit. If the output voltage being sensed at the VS1 pin exceeds the programmable threshold, the OVP flag is set; the response to that flag can be programmed. See Register 0x32 for more information.

UNDERVOLTAGE PROTECTION (UVP)

If the voltage being sensed at the VS1 pin goes below the programmable UVP threshold, the UVP flag is set. There are some exceptions to this (called undervoltage blanking), such as during startup. The response to the UVP condition is programmable. See Register 0x34 for more information.

CURRENT BALANCE (VOLT-SECOND BALANCE)

The ADP1043 has a dedicated circuit to maintain volt-second balance in the main transformer when operating in full-bridge topology. This means that a dc blocking capacitor is not necessary.

The circuit monitors the dc current flowing in both halves of the full bridge and stores this information. It compensates the PWM drive signals to ensure equal current flow in both halves of the full bridge. The input is through the CS1 pin. Several switching cycles are required for the circuit to operate effectively.

Note that the compensation of the PWM drive signals is performed on t_4 (OUTB) and t_8 (OUTD) only. Therefore, it is necessary to use these pins as the modulating PWM signals for the feature to operate correctly.

Also note that the ADP1043 assumes that the CS1 current pulse signal that it sees first in each cycle is related to OUTB, and that the second current pulse signal in each cycle is related to OUTD. If the first current pulse signal is smaller than the second, OUTB is increased and OUTD is decreased. If the first current pulse signal is greater than the second, OUTB is decreased and OUTD is increased.

POWER SUPPLY CALIBRATION AND TRIM

The ADP1043 is factory trimmed. The user cannot trim CS1, CS2, VS1, VS2, or VS3.

COMMUNICATION

I²C ADDRESS

Control of the ADP1043 is carried out via the I²C interface. The ADP1043 is connected to this bus as a slave device under the control of a master device.

The I²C address of the ADP1043 is set by connecting an external resistor from the ADD pin to AGND. Table 5 lists the recommended resistor values and the associated I²C addresses. Eight different addresses can be used. If an incorrect resistor value is used and the resulting I²C address is close to a threshold between two addresses, a flag is set (address flag in Register 0x03, Bit 5; see Table 10).

I²C Address 0x58 is the broadcast address, which allows multiple parts to be written to simultaneously. By using the broadcast address instead of a specific I²C address from Table 5, all ADP1043s on the I²C bus are written to. The broadcast address can be used for write commands only.

Table 5. Recommended Resistor Values for I²C Addresses

I²C Address	Resistor Value (kΩ)
0x50	9 (or connect the ADD pin directly to AGND)
0x51	27
0x52	45
0x53	63
0x54	81
0x55	98
0x56	116
0x57	134 (or connect the ADD pin directly to VDD)

GENERAL I²C TIMING

The I²C specification defines specific conditions for different types of read and write operations. General I²C read and write operations are shown in the timing diagrams of Figure 15, Figure 16, and Figure 17, and are described in this section.

The general I²C protocol operates as follows:

1. The master initiates a data transfer by establishing a start condition, defined as a high-to-low transition on the serial data line, SDA, while the serial clock line, SCL, remains high. This indicates that a data stream follows. All slave peripherals connected to the serial bus respond to the start condition and shift in the next 8 bits, consisting of a 7-bit slave address (MSB first) plus a R/$\overline{W}$ bit, which determines the direction of the data transfer, that is, whether data is written to or read from the slave device (0 = write, 1 = read).
2. The peripheral whose address corresponds to the transmitted address responds by pulling the data line low during the low period before the ninth clock pulse, known as the acknowledge bit, and holding it low during the high period of this clock pulse. All other devices on the bus remain idle while the selected device waits for data to be read from or written to it. If the R/$\overline{W}$ bit is a 0, the master writes to the slave device. If the R/$\overline{W}$ bit is a 1, the master reads from the slave device.
3. Data is sent over the serial bus in sequences of nine clock pulses: eight bits of data followed by an acknowledge bit from the slave device. Data transitions on the data line must occur during the low period of the clock signal and remain stable during the high period, because a low-to-high transition when the clock is high may be interpreted as a stop signal.
4. If the operation is a write operation, the first data byte after the slave address is a command byte that tells the slave device what to expect next. It may be an instruction, such as telling the slave device to expect a block write, or it may be a register address that tells the slave where subsequent data is to be written.
5. Because data can flow in only one direction, as defined by the R/$\overline{W}$ bit, it is not possible to send a command to a slave device during a read operation. Before a read operation, it may be necessary to first perform a write operation to tell the slave what sort of read operation to expect and/or the address from which data is to be read.
6. When all data bytes have been read or written, stop conditions are established. In write mode, the master pulls the data line high during the tenth clock pulse to assert a stop condition. In read mode, the master device releases the SDA line during the low period before the ninth clock pulse, but the slave device does not pull it low. This is known as a no acknowledge bit. The master then takes the data line low during the low period before the tenth clock pulse, then high during the tenth clock pulse to assert a stop condition.

Note that if several read or write operations must be performed in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

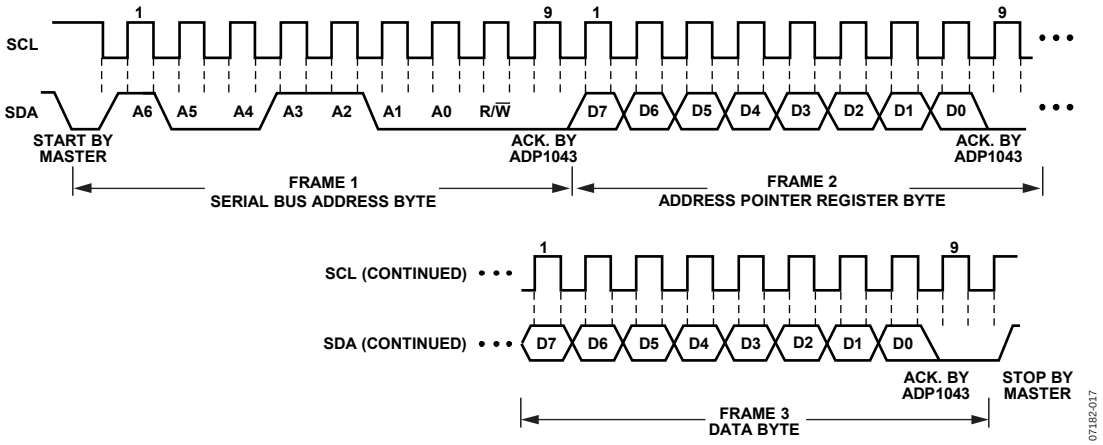

Figure 15. Writing a Register Address to the Address Pointer Register, Then Writing Data to the Selected Register

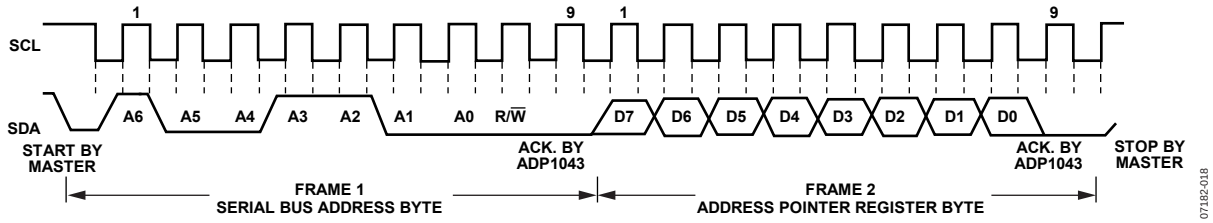

Figure 16. Writing to the Address Pointer Register Only

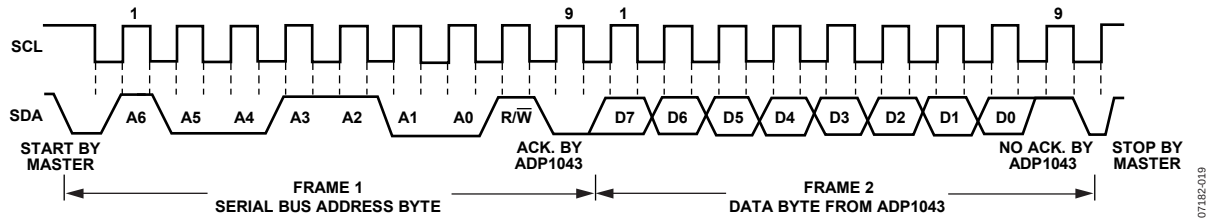

Figure 17. Reading Data from a Previously Selected Register

EEPROM OVERVIEW

The EEPROM is a CMOS page erase, 1024-byte (8 bits/byte) program embedded flash memory that is partitioned into two memory blocks: the main memory block and the information block. The information block is organized into 128 8-bit words. The information block is used by the ADP1043 for storing register contents and calibration coefficients. Only the information block is available for use.

Read EEPROM Contents

When power is first applied to VDD, the EEPROM contents are automatically downloaded from the EEPROM to the registers. The I²C interface does not communicate directly with the EEPROM (see Figure 18). Therefore, to read the EEPROM contents, the user must read the register contents at startup.

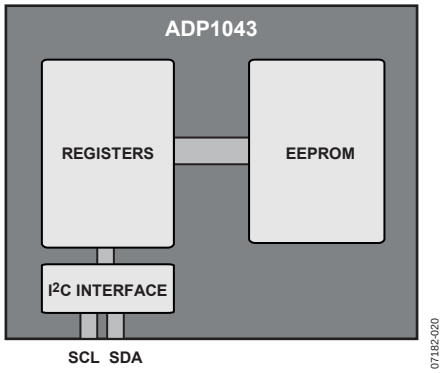

Figure 18. EEPROM and I²C Interface Configuration

Write EEPROM Contents

It is possible to write the entire register contents to the EEPROM by writing any value to Register 0x83. The I²C interface does not communicate directly with the EEPROM (see Figure 18). It simply uploads the register contents to the EEPROM. The Update EEPROM button on the Analog Devices software GUI performs this task.

Note that the EEPROM should not be written to for the first 500 ms after VDD has been applied.

EEPROM PASSWORD LOCK

The EEPROM password prevents the EEPROM contents from being changed accidentally or purposely by an unwanted source. The password ensures that critical specifications such as OVP and OCP cannot be changed.

The EEPROM is always locked. When the EEPROM downloads its contents to the registers, the password is also downloaded. If the user writes the same password to Register 0x68, the EEPROM is unlocked and can be updated. After the EEPROM is updated, it is locked again.

While the EEPROM is unlocked, it is possible to change the password by writing a new value to Register 0x68. After this value is updated, the EEPROM contains the new password. The factory default password is 0x00.

To update the EEPROM, the user must write to Register 0x83. Writing any value to this register updates the EEPROM.

EEPROM PASSWORD CHANGE

To change the EEPROM password, follow these steps:

1. Write the old password to Register 0x68 (password lock register).
2. Write the new password to Register 0x68 (password lock register) for the first time.
3. Write the new password to Register 0x68 (password lock register) for the second time.
4. Write the new password to Register 0x68 (password lock register) for the third time.
5. Write 0x00 to Register 0x83.

CYCLIC REDUNDANCY CHECK (CRC)

The ADP1043 performs a check to ensure that the EEPROM contents are correctly downloaded to registers at startup. It compares the total number of 1s downloaded with the total number of 1s that were last written to the EEPROM. If there is a discrepancy, the CRC fault flag is set in Register 0x03, Bit 1. This flag is used to ensure that the correct data is downloaded from the EEPROM to the registers at startup.

SOFTWARE GUI

A free software GUI is available for programming and configuring the ADP1043. The GUI is designed to be intuitive to power supply designers and dramatically reduces power supply design and development time. The software includes filter design and power supply PWM topology windows. The GUI is also an information center, displaying the status of all readings, monitoring, and flags on the ADP1043.

For more information about the GUI, contact Analog Devices for the latest software and a user's guide. Evaluation boards are also available by contacting Analog Devices.

REGISTER LISTING

Table 6. Register List

Address	Name
Fault Registers	
0x00	Fault Register 1
0x01	Fault Register 2
0x02	Fault Register 3
0x03	Fault Register 4
0x04	Latched Fault Register 1
0x05	Latched Fault Register 2
0x06	Latched Fault Register 3
0x07	Latched Fault Register 4
0x08	Fault Configuration Register 1
0x09	Fault Configuration Register 2
0x0A	Fault Configuration Register 3
0x0B	Fault Configuration Register 4
0x0C	Fault Configuration Register 5
0x0D	Fault Configuration Register 6
0x0E	Flag configuration
Value Registers	
0x10	First flag ID
0x11	First flag value
0x12	VS1/PWM value (input voltage)
0x13	CS1 value (input current)
0x14	CS1 × (VS1/PWM) value (input power)
0x15	VS1 voltage value
0x16	VS2 voltage value
0x17	Reserved
0x18	CS2 value (output current)
0x19	CS2 × VS3 value (output power)
0x1A	RTD temperature value
0x1D	Share bus value
0x1E	Modulation value
0x1F	Line impedance value
0x20	Reserved
Current Sense and Current Limit Registers	
0x21	Reserved
0x22	CS1 accurate OCP limit
0x23	CS2 gain trim
0x24	Reserved
0x25	Reserved
0x26	CS1 fast OCP blanking and CS2 OCP limit
0x27	CS1 fast OCP setting
0x28	Reserved
0x29	Reserved
0x2A	Share bus setting
0x2B	Temperature gain trim
0x2C	PSON/soft start setting
0x2D	Pin polarity setting
0x2E	Modulation limit
0x2F	OTP threshold
0x30	Reserved

Address	Name
Voltage Sense Registers	
0x31	VS3 voltage setting (remote voltage)
0x32	VS1 overvoltage limit (OVP)
0x33	Reserved
0x34	VS1 undervoltage limit (UVP)
0x35	Line impedance limit
0x36	Load line impedance
0x38	Reserved
0x39	Reserved
0x3A	Reserved
0x3B	Reserved
0x3C	Reserved
ID Registers	
0x3D	Manufacturer ID
0x3E	Device ID
PWM and Synchronous Rectification Timing Registers	
0x3F	OUTAUX switching frequency setting
0x40	PWM switching frequency setting
0x41	OUTA positive edge timing (OUTA pin)
0x42	OUTA positive edge setting (OUTA pin)
0x43	OUTA negative edge timing (OUTA pin)
0x44	OUTA negative edge setting (OUTA pin)
0x45	OUTB positive edge timing (OUTB pin)
0x46	OUTB positive edge setting (OUTB pin)
0x47	OUTB negative edge timing (OUTB pin)
0x48	OUTB negative edge setting (OUTB pin)
0x49	OUTC positive edge timing (OUTC pin)
0x4A	OUTC positive edge setting (OUTC pin)
0x4B	OUTC negative edge timing (OUTC pin)
0x4C	OUTC negative edge setting (OUTC pin)
0x4D	OUTD positive edge timing (OUTD pin)
0x4E	OUTD positive edge setting (OUTD pin)
0x4F	OUTD negative edge timing (OUTD pin)
0x50	OUTD negative edge setting (OUTD pin)
0x51	SR1 positive edge timing (SR1 pin)
0x52	SR1 positive edge setting (SR1 pin)
0x53	SR1 negative edge timing (SR1 pin)
0x54	SR1 negative edge setting (SR1 pin)
0x55	SR2 positive edge timing (SR2 pin)
0x56	SR2 positive edge setting (SR2 pin)
0x57	SR2 negative edge timing (SR2 pin)
0x58	SR2 negative edge setting (SR2 pin)
0x59	OUTAUX positive edge timing (OUTAUX pin)
0x5A	OUTAUX positive edge setting (OUTAUX pin)
0x5B	OUTAUX negative edge timing (OUTAUX pin)
0x5C	OUTAUX negative edge setting (OUTAUX pin)
0x5D	OUTx and SRx pin disable setting

Address	Name
Digital Filter Programming Registers	
0x60	Normal mode digital filter LF gain setting
0x61	Normal mode digital filter zero setting
0x62	Normal mode digital filter pole setting
0x63	Normal mode digital filter HF gain setting
0x64	Reserved
0x65	Reserved
0x66	Reserved
0x67	Reserved
0x68	Password lock

DETAILED REGISTER DESCRIPTIONS

FAULT REGISTERS

Register 0x04 to Register 0x07 are latched fault registers. In these registers, flags are not reset when the fault disappears. Flags are cleared only by a register read (provided that the fault no longer persists). Note that latched bits are clocked on a low-to-high transition only. Also note that these register bits are cleared when read via the I²C interface unless the fault is still present. It is recommended that the latched fault register be read again after the faults disappear to ensure that the register is reset.

Table 7. Register 0x00—Fault Register 1 and Register 0x04—Latched Fault Register 1 (1 = Fault, 0 = Normal Operation)

Bit	Name	R/W	Description	Register	Action
7	Power supply	R	1 = power supply is off. All PWM outputs are disabled. This bit stays high until the power supply is restarted.		None
6	GATE	R	1 = control signal at the GATE pin (Pin 16) is off.		None
5	PGOOD1 fault	R	1 = Power-Good 1 fault. At least one of the following is out of range: CS1 OCP, CS2 OCP, VS1 OVP, or UVP.		None
4	PGOOD2 fault	R	1 = Power-Good 2 fault. Any of the following flags has been set: power supply, GATE, fast OCP (CS1), CS1 OCP, CS2 OCP, voltage continuity, UVP, VDD UV, VCORE OV, VDD OV, VS1 OVP, OTP, CRC fault, EEPROM unlocked.		None
3	SR off	R	Sync rects are disabled. This flag is set when one of the following cases is true: SR1 and SR2 are disabled by the user. A flag that was configured to disable the sync rects has been set.	 0x5D 0x08 to 0x0E	None
2	Fast OCP (CS1)	R	CS1 current is above its fast overcurrent protection limit. This is a 1.2 V threshold on the CS1 pin. Fast OCP is a comparator.		Programmable
1	CS1 OCP	R	CS1 current is above its accurate overcurrent protection limit.	0x22	Programmable
0	CS2 OCP	R	CS2 current is above its accurate overcurrent protection limit.	0x26	Programmable

Table 8. Register 0x01—Fault Register 2 and Register 0x05—Latched Fault Register 2 (1 = Fault, 0 = Normal Operation)

Bit	Name	R/W	Description	Register	Action
7	Voltage continuity	R	Voltage differential between VS1 and VS2 pins or between VS2 and VS3 pins is outside limits. Either (VS1 − VS2) > 100 mV or (VS2 − VS3) > 100 mV.		Programmable
6	UVP	R	VS1 is below its undervoltage limit.	0x34	Programmable
5	Reserved	R	Reserved.		
4	VDD UV	R	VDD is below limit.		Immediate shutdown
3	VCORE OV	R	2.5 V VCORE is above limit.		Immediate shutdown
2	VDD OV	R	VDD is above limit. The I²C interface stays functional, but a PSON toggle is required to restart the power supply.		Immediate shutdown
1	Reserved	R	Reserved.		
0	VS1 OVP	R	VS1 is above its overvoltage limit.	0x32	Programmable

Table 9. Register 0x02—Fault Register 3 and Register 0x06—Latched Fault Register 3 (1 = Fault, 0 = Normal Operation)

Bit	Name	R/W	Description	Register	Action
7	OTP	R	Temperature is above OTP limit.	0x2F	Programmable
6	Reserved	R	Reserved.		
5	Share bus	R	Current share is outside regulation limit.	0x2A	Programmable
[4:3]	Reserved	R	Reserved.		
2	Line impedance	R	Line impedance between VS2 and VS3 is above limit.	0x35	None
1	Reserved	R	Reserved.		
0	External flag	R	The external flag pin (FLAGIN) is set.		Programmable

Table 10. Register 0x03—Fault Register 4 and Register 0x07—Latched Fault Register 4 (1 = Fault, 0 = Normal Operation)

Bit	Name	R/W	Description	Register	Action
7	Reserved	R	Reserved.		
6	Modulation	R	Modulation is at its minimum or maximum limit.	0x2E	None
5	Address	R	The ADD resistor is not correct.		None
[4:2]	Reserved	R	Reserved.		
1	CRC fault	R	The EEPROM contents downloaded are incorrect.		None
0	EEPROM unlocked	R	The EEPROM is unlocked.		None

Table 11. Register 0x08 to Register 0x0D—Fault Configuration Registers

Register Name	Address	Bit	Flag	Shutdown Debounce
Fault Configuration Register 1	0x08	[7:4]	CS1 fast OCP	See Register 0x27
		[3:0]	CS1 accurate OCP	See Register 0x0E
Fault Configuration Register 2	0x09	[7:4]	CS2 accurate OCP	See Register 0x0E
		[3:0]	Voltage sense	100 ms
Fault Configuration Register 3	0x0A	[7:4]	UVP	100 ms
		[3:0]	Reserved	
Fault Configuration Register 4	0x0B	[7:4]	Reserved	
		[3:0]	Local OVP (VS1)	100 ms
Fault Configuration Register 5	0x0C	[7:4]	OTP	100 ms
		[3:0]	Share bus	100 ms
Fault Configuration Register 6	0x0D	[7:4]	External flag input (FLAGIN)	100 ms
		[3:0]	Reserved	

Register 0x08 to Register 0x0D allow the user to program the response when each flag is set.

Table 12. Register 0x08 to Register 0x0D—Fault Configuration Register Bit Descriptions

Bit	Name	R/W	Description		
7	Timing	R/W	This bit specifies when the flag is set. 0 = after debounce. 1 = immediately.		
6	Resolve issue	R/W	This bit specifies when the part is reenabled after the fault that triggered the flag has been resolved. 0 = reenable 1 sec after flag is reset. 1 = remain disabled; power supply must be restarted to reenable.		
[5:4]	Action	R/W	These bits specify the action that the part takes in response to the flag.		
			Bit 5	**Bit 4**	**Action**
			0	0	Ignore flag completely
			0	1	Disable sync rect
			1	0	Disable GATE
			1	1	Disable power supply (disable all PWMs and GATE)
3	Timing	R/W	Same as Bit 7.		
2	Resolve issue	R/W	Same as Bit 6.		
[1:0]	Action	R/W	Same as Bits[5:4].		

Table 13. Register 0x0E—Flag Configuration Register Bit Descriptions

Bit	Name	R/W	Description			
[7:5]	Reserved	R/W	Reserved.			
[4:2]	Accurate OCP off debounce for CS1 and CS2	R/W	When an accurate OCP flag is set, there is a debounce before that flag's action is performed. This debounce is programmed using these bits.			
			Bit 4	**Bit 3**	**Bit 2**	**Debounce**
			0	0	0	1.3 ms
			0	0	1	13 ms
			0	1	0	130 ms
			0	1	1	260 ms
			1	0	0	600 ms
			1	0	1	1.3 sec
			1	1	0	2 sec
			1	1	1	2.6 sec
[1:0]	Flag reenable time	R/W	These bits specify the amount of time that the part must wait to be reenabled after the fault that triggered the flag has been resolved.			
			Bit 1	**Bit 0**	**Time (sec)**	
			0	0	0.5	
			0	1	1	
			1	0	2	
			1	1	4	

VALUE REGISTERS

Table 14. Register 0x10—First Flag ID

Bit	Name	R/W	Description						
[7:6]	Reserved	R	Reserved.						
5	First flag	R	If this bit = 0, no flag is set. If this bit = 1, a flag is set, and the first flag ID can be read from Bits[4:0].						
[4:0]	First flag ID	R	These bits record which flag was set first. Restarting the power supply resets this register.						
			Bit 4	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Flag**	**Error**
			0	0	0	0	0	Register 0x00, Bit 0	CS2 accurate OCP
			0	0	0	0	1	Register 0x00, Bit 1	CS1 accurate OCP
			0	0	0	1	0	Register 0x00, Bit 2	CS1 fast OCP
			0	0	0	1	1	Register 0x00, Bit 3	SR OFF
			…	…	…	…	…	….	…
			1	1	1	0	1	Register 0x03, Bit 5	Address
			1	1	1	1	0	Register 0x03, Bit 6	Modulation
			1	1	1	1	1	Register 0x03, Bit 7	Reserved

Table 15. Register 0x11—First Flag Value

Bit	Name	R/W	Description
[7:0]	First flag value	R	This 8-bit register contains the contents of the first flag that caused the power supply to fail. For example, if CS1 OCP caused the power supply to fail, this register contains the CS1 current value at the time of failure. If the first flag has no associated value, this register reads 0x00. For example, if the first flag is an external flag, this register reads 0x00.

Table 16. Register 0x12—VS1/PWM Value (Input Voltage)

Bit	Name	R/W	Description
[15:0]	Input voltage value	R	This register contains the 16-bit input voltage information. Because the input voltage is normally on the other side of the isolation barrier from the ADP1043, the part does not directly sense the input voltage. The input voltage is defined as the VS1 voltage divided by the PWM modulation. To read the input voltage information, this register must be read twice. The eight bits of the first read return the eight MSBs of the input voltage information. The eight bits of the second read return the eight LSBs of the input voltage information. To translate this reading into the real input voltage, use the following equation: $V_{INPUT} = (Input\_Voltage\_Value\_Reading/2592) \times ((R1 + R2)/R2)$ where *R1* and *R2* are the external resistor divider values between the power supply output and the VS1 pin. This reading does not take into account an external turns ratio on the main transformer.

Table 17. Register 0x13—CS1 Value (Input Current)

Bit	Name	R/W	Description
[15:4]	Input current value	R	This register contains the 12-bit input current information. This value is derived from a voltage measurement at the CS1 input. To read the input current information, this register must be read twice. The eight bits of the first read return the eight MSBs of the input current information. The top four bits of the second read return the four LSBs of the input current information. The range of the CS1 input pin is from 0 V to 1.58 V. It has 12 bits of resolution, which results in an LSB size of 386 µV. At 0 V input, the value in this register is 0 (0x000). At 1.5 V input, the value in this register is 3888 (0xF30). At 1 V input, the value in this register is 2592 (0xA20).
[3:0]	Reserved	R	Reserved.

Table 18. Register 0x14—CS1 × (VS1/PWM) Value (Input Power)

Bit	Name	R/W	Description
[15:0]	Input power value	R	This register contains the 16-bit input power information. This value is the product of the input voltage (VS1/PWM) multiplied by the input current (CS1), that is, (VS1/PWM) × CS1. To read the input power information, this register must be read twice. The eight bits of the first read return the eight MSBs of the input power information. The eight bits of the second read return the eight LSBs of the input power information.

Table 19. Register 0x15—VS1 Voltage Value

Bit	Name	R/W	Description
[15:4]	VS1 voltage value	R	This register contains the 12-bit local output voltage information. This voltage is measured at the VS1 pin. To read the VS1 voltage information, this register must be read twice. The eight bits of the first read return the eight MSBs of the local output information. The top four bits of the second read return the four LSBs of the local output voltage information. The range of the VS1 input pin is from 0 V to 1.58 V. It has 12 bits of resolution, which results in an LSB size of 386 µV. At 0 V input, the value in this register is 0 (0x000). At 1.5 V input, the ADC output is 3888 (0xF30). The recommended nominal voltage at this pin is 1 V. At 1 V input, the value in this register is 2592 (0xA20).
[3:0]	Reserved	R	Reserved.

Table 20. Register 0x16—VS2 Voltage Value

Bit	Name	R/W	Description
[15:4]	VS2 voltage value	R	This register contains the 12-bit local output voltage information. This voltage is measured at the VS2 pin. To read the VS2 voltage information, this register must be read twice. The eight bits of the first read return the eight MSBs of the local output information. The top four bits of the second read return the four LSBs of the local output voltage information. The range of the VS2 input pin is from 0 V to 1.58 V. It has 12 bits of resolution, which results in an LSB size of 386 µV. At 0 V input, the value in this register is 0 (0x000). At 1.5 V input, the ADC output is 3888 (0xF30). The recommended nominal voltage at this pin is 1 V. At 1 V input, the value in this register is 2592 (0xA20).
[3:0]	Reserved	R	Reserved.

Table 21. Register 0x18—CS2 Value (Output Current)

Bit	Name	R/W	Description
[15:4]	Output current value	R	This register contains the 12-bit output current information. This information is the voltage drop across the sense resistor. The user must divide this value by the sense resistor value to obtain the current value. To read the output current information, this register must be read twice. The eight bits of the first read return the eight MSBs of the output current information. The top four bits of the second read return the four LSBs of the output current information. The relationship of the current sensing voltage and the ADC output value is determined by the nominal voltage setting in Bits[7:6] of Register 0x23. If the nominal voltage is from 75 mV to 150 mV, the full range voltage is 225 mV with an ADC value of 0xFFF. At 150 mV, the value in this register is 0x99A. If the nominal voltage is from 37.5 mV to 75 mV, the full range voltage is 125 mV with an ADC value of 0xFFF. At 75 mV, the value in this register is 0x99A. If the nominal voltage is from 0 mV to 37.5 mV, the full range voltage is 62.5 mV with an ADC value of 0xFFF. At 37.5 mV, the value in this register is 0x99A.
[3:0]	Reserved	R	Reserved.

Table 22. Register 0x19—CS2 × VS3 Value (Output Power)

Bit	Name	R/W	Description
[15:0]	Output power value	R	This register contains the 16-bit output power information. This value is the product of the remote output voltage value (VS3) and the output current reading (CS2). To read the output power information, this register must be read twice. The eight bits of the first read return the eight MSBs of the output power information. The eight bits of the second read return the eight LSBs of the output power information.

Table 23. Register 0x1A—RTD Temperature Value

Bit	Name	R/W	Description
[15:4]	Temperature value	R	This register contains the 12-bit output temperature information, as determined from the RTD pin. To read the temperature information, this register must be read twice. The eight bits of the first read return the eight MSBs of the temperature information. The top four bits of the second read return the four LSBs of the temperature information.
[3:0]	Reserved	R	Reserved.

Table 24. Register 0x1D—Share Bus Value

Bit	Name	R/W	Description
[7:0]	Share bus value	R	This register contains the 8-bit share bus voltage information. If the power supply is the master, this register outputs 0.

Table 25. Register 0x1E—Modulation Value

Bit	Name	R/W	Description
[7:0]	Modulation value	R	This register contains the 8-bit modulation information. It outputs the amount of modulation from 0% to 100% that is being placed on the modulating edges.

Table 26. Register 0x1F—Line Impedance Value

Bit	Name	R/W	Description
[7:0]	Line impedance value	R	This register contains the 8-bit line impedance information. This value is (VS2 − VS3)/CS2.

CURRENT SENSE AND CURRENT LIMIT REGISTERS

Table 27. Register 0x22—CS1 Accurate OCP Limit

Bit	Name	R/W	Description
[7:0]	CS1 accurate OCP	R/W	This register sets the CS1 accurate OCP current level. This 8-bit number is compared to the CS1 value register (Register 0x13). If the CS1 value register is greater than the number in this register, the CS1 accurate OCP flag is set. This register can be set to a value from 0 to 254 (0xFE); setting this register to 255 (0xFF) is not allowed. The range of these bits is 6.17 mV to 1.57 V in steps of 6.17 mV. The following equation gives the threshold of the CS1 OCP: *CS1_OCP_Threshold* = [(1 + *CS1_Accurate_OCP_Setting*)/256)] × 1.58 V.

Table 28. Register 0x23—CS2 Gain Trim

Bit	Name	R/W	Description		
[7:6]	CS2 nominal	R/W	These bits set the nominal full load voltage drop across the sense resistor. This register contains factory calibrated settings. If changing Bits[7:6], the user must ensure that the contents of Bits[5:0] not be changed.		
			Bit 7	**Bit 6**	**Nominal Voltage Drop Across R_{SENSE} at Full Load**
			0	0	37.5 mV
			0	1	75 mV
			1	0	150 mV
			1	1	150 mV
[5:0]	Reserved	R/W	These bits contain factory calibrated settings. If changing Bits[7:6], the user must ensure that the contents of Bits[5:0] not be changed.		

Table 29. Register 0x26—CS1 Fast OCP Blanking and CS2 OCP Limit

Bit	Name	R/W	Description			
[7:5]	CS1 fast OCP blanking	R/W	These bits determine the blanking time for CS1 before fast OCP is enabled. This time is measured from the start of a switching cycle. It is synchronized with the rising edge of OUTB and OUTD. If using OUTAUX, the time is synchronized with the rising edge of OUTAUX.			
			Bit 7	**Bit 6**	**Bit 5**	**Delay (ns)**
			0	0	0	40
			0	0	1	40
			0	1	0	80
			0	1	1	120
			1	0	0	200
			1	0	1	400
			1	1	0	600
			1	1	1	800
[4:0]	CS2 accurate OCP setting	R/W	These bits set the CS2 OCP threshold from 0 to 2976 (0xBA0). The digital word that is output from the CS2 ADC is compared with this threshold. If the CS2 ADC reading (Register 0x18) is greater than the OCP threshold, the CS2 OCP flag is set. Setting all bits to 1 results in the maximum current limit (2976). Each LSB increases the OCP limit by 93 (0x5D). Another way to calculate this threshold is in terms of mV. The range of these bits is 1 mV to 183 mV in 5.68 mV steps. The following equation gives the threshold of the CS2 OCP. If the voltage drop across the CS2 pins is greater than this threshold, the CS2 accurate OCP flag is set. *CS2_OCP_Threshold* (mV) = [(1 + (*CS2_Accurate_OCP_Setting* × 6))/256] × 250			

Table 30. Register 0x27—CS1 Fast OCP Setting

Bit	Name	R/W	Description		
[7:6]	CS1 fast OCP debounce	R/W	These bits set the CS1 debounce value. This is the minimum time that the CS1 signal must be constantly above the fast OCP limit before it shuts down the PWMs. When this happens, all PWMs are disabled for the remainder of the switching cycle.		
			Bit 7	**Bit 6**	**Debounce (ns)**
			0	0	0
			0	1	40
			1	0	80
			1	1	120
5	Current balance	R/W	Setting this bit enables current balance for the main transformer (used for full-bridge configurations). This value introduces extra modulation on the OUTB and OUTD modulating waveforms to provide current balance in both branches of the full bridge. For more information, see the Current Balance (Volt-Second Balance) section.		
4	CS1 fast OCP bypass	R/W	Setting this bit to 1 means that the FLAGIN pin is used for CS1 fast OCP instead of the CS1 pin.		
[3:2]	Reserved	R/W	Reserved.		
[1:0]	CS1 fast OCP timeout	R/W	If the CS1 fast OCP comparator is set, all PWMs are immediately disabled for the remainder of the switching cycle. The PWMs resume normal operation at the beginning of the next switching cycle. These bits set the number of consecutive switching cycles for the comparator before the CS1 fast OCP flag is set.		
			Bit 1	**Bit 0**	**Number of Switching Cycles**
			0	0	1
			0	1	2
			1	0	4
			1	1	4

Table 31. Register 0x2A—Share Bus Setting

Bit	Name	R/W	Description		
7	Reserved	R/W	Reserved.		
6	Primary or secondary share	R/W	0 = current sharing is performed from the CS2 input signal. 1 = current sharing is performed from the CS1 input signal.		
[5:3]	Reserved	R/W	Set these bits to 0 for normal operation.		
[2:1]	Current share voltage capture	R/W	These bits set how high the power supply output voltage can go above nominal as it attempts to provide more power to the load so that it is sharing correctly.		
			Bit 2	**Bit 1**	**Option**
			0	0	1%
			0	1	2%
			1	0	3%
			1	1	4%
0	Reserved	R/W	Reserved.		

Table 32. Register 0x2B—Temperature Gain Trim

Bit	Name	R/W	Description
[7:5]	Reserved	R/W	Set these bits to 0 for normal operation.
4	Gain polarity	R/W	1 = negative gain is introduced. 0 = positive gain is introduced.
[3:0]	Gain trim	R/W	This register calibrates the RTD ADC gain. It calibrates for errors in the ADC. This allows ±12% trim to be realized.

Table 33. Register 0x2C—PSON/Soft Start Setting

Bit	Name	R/W	Description		
[7:6]	PGOOD1 on delay	R/W	At startup, there is a delay (t_5) before PGOOD1 is enabled. PGOOD1 is not enabled until a period of time after the following signals are all within normal limits: CS1 OCP, CS2 OCP, VS1 OVP, and UVP. These bits set Time t_5.		
			Bit 7	**Bit 6**	**Delay (ms)**
			0	0	400
			0	1	200
			1	0	800
			1	1	1600
[5:4]	PGOOD1 off delay	R/W	When PSON is disabled, there is a delay before PGOOD1 is disabled. This delay is programmed using these bits.		
			Bit 5	**Bit 4**	**Delay (ms)**
			0	0	400
			0	1	200
			1	0	800
			1	1	1600
3	Reserved	R/W	Reserved.		
2	Soft stop enable	R/W	1: soft stop time = soft start time 0: no active discharge time		
[1:0]	Soft start	R/W	These bits set the soft start ramp time, that is, the amount of time that it takes for the power supply to reach its nominal value.		
			Bit 1	**Bit 0**	**Rise Time**
			0	0	360 µs
			0	1	10 ms
			1	0	20 ms
			1	1	40 ms

Table 34. Register 0x2D—Pin Polarity Setting

Bit	Name	R/W	Description		
[7:6]	PSON delay time	R/W	These bits set Time t_1, which is the delay from when the PSON signal is enabled to when the soft start begins.		
			Bit 7	**Bit 6**	**Delay Time (sec)**
			0	0	0
			0	1	0.5
			1	0	1
			1	1	2
5	PGOOD2 polarity	R/W	This bit sets the polarity of the PGOOD2 output pin: 1 = inverted (low = on).		
4	Software PSON	R/W	0 = power supply off. 1 = power supply on.		
3	PSON select	R/W	0 = software PSON. If this bit is set to 0, the software PSON bit (Bit 4) is used as the control signal to turn the power supply on and off. 1 = hardware PSON. If this bit is set to 1, the PSON input pin is used as the control signal to turn the power supply on and off.		
2	PGOOD1 polarity	R/W	This bit sets the polarity of the PGOOD1 output pin: 1 = inverted (low = on).		
1	GATE polarity	R/W	This bit sets the polarity of the GATE control pin: 1 = inverted (low = on).		
0	PSON polarity	R/W	This bit sets the polarity of the PSON input pin: 1 = inverted (low = on).		

Table 35. Register 0x2E—Modulation Limit

Bit	Name	R/W	Description				
7	Full bridge	R/W	Set this bit to 1 when operating in full-bridge mode. This mode distributes the modulation equally between two PWMs instead of one. It affects the modulation high limit and the modulation low limit settings.				
[6:4]	Modulation high limit	R/W	This value sets the maximum allowed modulation that can be applied to a PWM. The value is a percentage of the switching period.				
			Bit 6	**Bit 5**	**Bit 4**	**High Limit (%)**	**Limit (%) in Full-Bridge Mode**
			0	0	0	Nominal + 12.5%	Nominal + 6.25%
			0	0	1	Nominal + 25%	Nominal + 12.5%
			0	1	0	Nominal + 31.25%	Nominal + 15.625%
			0	1	1	Nominal + 37.5%	Nominal + 18.75%
			1	0	0	Nominal + 43.75%	Nominal + 21.875%
			1	0	1	Nominal + 46.88%	Nominal + 23.44%
			1	1	0	Nominal + 48.44%	Nominal + 24.22%
			1	1	1	Nominal + 50%	Nominal + 25%
3	Reserved	R/W	Reserved.				
2	Pulse skipping	R/W	Setting this bit enables pulse skipping mode. If the ADP1043 requires a duty cycle lower than the modulation low limit, pulse skipping is enabled.				
[1:0]	Modulation low limit	R/W	This value sets the minimum allowed modulation that can be applied to a PWM. If the modulation calculated is to be lower than this limit, pulse skipping can be enabled.				
			Bit 1	**Bit 0**	**Low Limit (%)**	**Limit (%) in Full-Bridge Mode**	
			0	0	Nominal – 50%	Nominal – 25%	
			0	1	Nominal – 48.44%	Nominal – 24.22%	
			1	0	Nominal – 46.88%	Nominal – 23.44%	
			1	1	Nominal – 43.75%	Nominal – 21.875%	

Table 36. Register 0x2F—OTP Threshold

Bit	Name	R/W	Description
[7:0]	OTP threshold	R/W	This value is compared to the RTD ADC reading (Register 0x1A). If the RTD ADC reading is lower than the threshold set in this register, the OTP flag is set. The flag is set below the threshold because using an NTC thermistor causes the reading to decrease as the temperature increases. Each LSB typically corresponds to an increased OTP threshold of 3 mV. The RTD ADC range is 0 V to 1.58 V; the OTP threshold is 10 mV to 775 mV. There is a hysteresis of 16 mV on the OTP flag.

Bit 7	Bit 6	….	Bit 3	Bit 2	Bit 1	Bit 0	OTP Limit (mV)
0	0	….	0	0	1	1	9.3
0	0	….	0	1	0	0	12.4
0	0	….	0	1	0	1	15.5
…..	…..	….	….	….	…..	….	…..
1	1	1	1	0	0	1	771.9
1	1	1	1	0	1	0	775

VOLTAGE SENSE REGISTERS

Table 37. Register 0x31—VS3 Voltage Setting (Remote Voltage)

Bit	Name	R/W	Description
[7:0]	VS3 voltage setting	R/W	This register is used to set the remote voltage (voltage differential at the VS3+ and VS3− pins). Programmable from 0% to 158% of nominal voltage. Each LSB corresponds to a 0.6% increase.

Table 38. Register 0x32—VS1 Overvoltage Limit (OVP)

Bit	Name	R/W	Description
[7:4]	VS1 OVP setting	R/W	Local overvoltage limit. This limit is programmable from 110% to 128% of the nominal VS1 voltage; 0x00 corresponds to 110%. Each LSB results in an increase of 1.23%. The range is 0 to 15 (1.1 V to 1.28 V in steps of 11.25 mV). The VS1 OVP threshold is calculated as follows: *VS1_OVP_Threshold* = [(89 + *VS1_OVP_Setting*)/128] × 1.58 V.
[3:2]	Reserved	R/W	Reserved.
[1:0]	OVP sampling	R/W	The OVP flag is set if the average voltage during the OVP sampling period is greater than the OVP threshold. This OVP flag sampling period is 80 µs. The number of samples can be increased using these bits. If the number of samples is increased, the average voltage must be greater than the OVP threshold for each of those cycles. For example, if this value is set to two cycles, the average voltage must be greater than the OVP threshold for both cycles.

Bit 1	Bit 0	Additional Sampling (µs)
0	0	0 (one sample can set the OVP flag)
0	1	80 (two samples set the OVP flag)
1	0	160 (three samples set the OVP flag)
1	1	240 (four samples set the OVP flag)

Table 39. Register 0x34—VS1 Undervoltage Limit (UVP)

Bit	Name	R/W	Description
[7:4]	Reserved	R/W	Reserved.
[3:0]	VS1 UVP setting	R/W	These bits set the UVP limit. UVP is ignored during soft start. This limit can be programmed from 84% to 100% of the nominal VS1 voltage (1 V). Each LSB increases the voltage by 1%. The range is 0 to 15 (0.84 V to 1.025 V in steps of 5.9 mV). The VS1 UVP threshold is calculated as follows: *VS1_UVP_Threshold* = [(68 + *VS1_UVP_Setting*)/128] × 1.58 V.

Table 40. Register 0x35—Line Impedance Limit

Bit	Name	R/W	Description
[7:0]	Line impedance limit	R/W	This value sets the threshold at which the line impedance flag is enabled. This 8-bit value is compared with the line impedance value (Register 0x1F). If the line impedance value exceeds this value, the line impedance flag is set (Register 0x02, Bit 2).

Table 41. Register 0x36—Load Line Impedance

Bit	Name	R/W	Description			
[7:4]	Reserved	R/W	Reserved.			
3	Enable	R/W	Set this bit to enable the load line.			
[2:0]	Load line	R/W	This value specifies how much the output voltage decreases from nominal at full load. For example, a 12 V system programmed with an 8% load line means that the output voltage varies from 12 V at no load to 11.04 V at 100% load.			
			Bit 2	**Bit 1**	**Bit 0**	**Impedance Setting**
			0	0	0	128%
			0	0	1	64%
			0	1	0	32%
			0	1	1	16%
			1	0	0	8%
			1	0	1	4%
			1	1	0	2%
			1	1	1	1%

ID REGISTERS

Table 42. Register 0x3D—Manufacturer ID (Power-On Default: 0x41)

Bit	Name	R/W	Description
[7:0]	Manufacturer ID code	R	This register contains the manufacturer's ID code for the device. It is used by the manufacturer for test purposes and should not be read from or written to in normal operation. This value is hardwired to 0x41, the Analog Devices ID code.

Table 43. Register 0x3E—Device ID (Power-On Default: 0x43)

Bit	Name	R/W	Description
[7:0]	Device ID code	R	This register contains the ID code for the device. This value is hardwired to 0x43 to represent the ADP1043.

PWM AND SYNC RECT TIMING REGISTERS

Figure 19 and Register 0x3F to Register 0x5D describe the implementation and programming of the seven PWM signals that are output from the ADP1043. In general, it is recommended that t_1 be set to 0 and that t_1 be set as the reference point for the other signals.

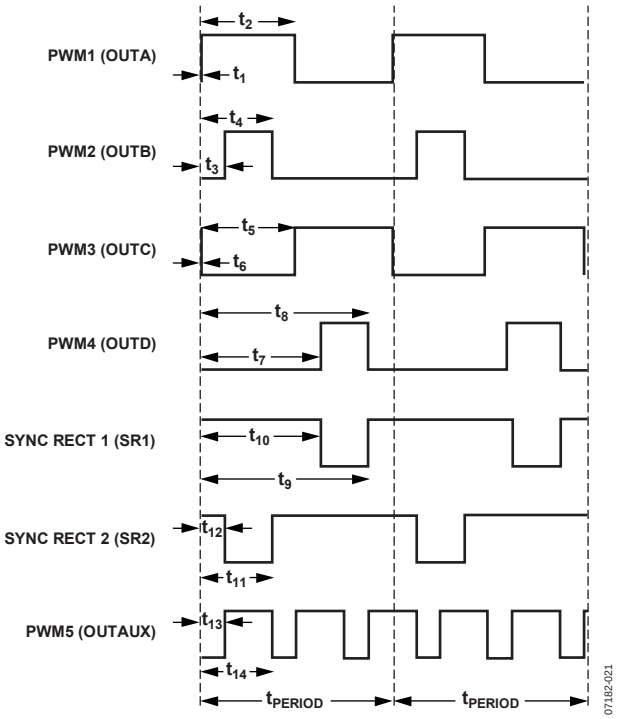

Figure 19. PWM Timing Diagram

Table 44. Register 0x3F—OUTAUX Switching Frequency Setting

Bit	Name	R/W	Description						
[7:6]	Reserved	R/W	Reserved.						
[5:0]	Switching frequency	R/W	This register sets the switching frequency of the OUTAUX signal.						
			Bit 5	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Frequency (kHz)**
			0	0	0	0	0	0	48.8
			0	0	0	0	0	1	50.4
			0	0	0	0	1	0	52
			0	0	0	0	1	1	53.8
			0	0	0	1	0	0	55.8
			0	0	0	1	0	1	57.9
			0	0	0	1	1	0	60.1
			0	0	0	1	1	1	62.5
			0	0	1	0	0	0	65.1
			0	0	1	0	0	1	67.9
			0	0	1	0	1	0	71
			0	0	1	0	1	1	74.4
			0	0	1	1	0	0	78.1
			0	0	1	1	0	1	82.2
			0	0	1	1	1	0	86.8
			0	0	1	1	1	1	91.9
			0	1	0	0	0	0	97.6
			0	1	0	0	0	1	100.8
			0	1	0	0	1	0	104.1
			0	1	0	0	1	1	107.7
			0	1	0	1	0	0	111.6

Bit	Name	R/W	Description						
[5:0]	Switching frequency	R/W	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Frequency (kHz)**
			0	1	0	1	0	1	115.7
			0	1	0	1	1	0	120.2
			0	1	0	1	1	1	125
			0	1	1	0	0	0	130.2
			0	1	1	0	0	1	135.8
			0	1	1	0	1	0	142
			0	1	1	0	1	1	148.8
			0	1	1	1	0	0	156.2
			0	1	1	1	0	1	164.5
			0	1	1	1	1	0	173.6
			0	1	1	1	1	1	183.8
			1	0	0	0	0	0	195.3
			1	0	0	0	0	1	201.6
			1	0	0	0	1	0	208.3
			1	0	0	0	1	1	215.5
			1	0	0	1	0	0	223.2
			1	0	0	1	0	1	231.5
			1	0	0	1	1	0	240.4
			1	0	0	1	1	1	250
			1	0	1	0	0	0	260
			1	0	1	0	0	1	271
			1	0	1	0	1	0	284
			1	0	1	0	1	1	297
			1	0	1	1	0	0	312
			1	0	1	1	0	1	328
			1	0	1	1	1	0	347
			1	0	1	1	1	1	367
			1	1	0	0	0	0	390
			1	1	0	0	0	1	416
			1	1	0	0	1	0	446
			1	1	0	0	1	1	480
			1	1	0	1	0	0	521
			1	1	0	1	0	1	568
			1	1	0	1	1	0	625

Table 45. Register 0x40—PWM Switching Frequency Setting

Bit	Name	R/W	Description						
[7:6]	Reserved	R/W	Reserved.						
[5:0]	Switching frequency	R/W	This register sets the switching frequency of the PWM pins.						
			Bit 5	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Frequency (kHz)**
			0	0	0	0	0	0	48.8
			0	0	0	0	0	1	50.4
			0	0	0	0	1	0	52
			0	0	0	0	1	1	53.8
			0	0	0	1	0	0	55.8
			0	0	0	1	0	1	57.9
			0	0	0	1	1	0	60.1
			0	0	0	1	1	1	62.5
			0	0	1	0	0	0	65.1
			0	0	1	0	0	1	67.9

Bit	Name	R/W	Description						
[5:0]	Switching frequency	R/W	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**	**Frequency (kHz)**
			0	0	1	0	1	0	71
			0	0	1	0	1	1	74.4
			0	0	1	1	0	0	78.1
			0	0	1	1	0	1	82.2
			0	0	1	1	1	0	86.8
			0	0	1	1	1	1	91.9
			0	1	0	0	0	0	97.6
			0	1	0	0	0	1	100.8
			0	1	0	0	1	0	104.1
			0	1	0	0	1	1	107.7
			0	1	0	1	0	0	111.6
			0	1	0	1	0	1	115.7
			0	1	0	1	1	0	120.2
			0	1	0	1	1	1	125
			0	1	1	0	0	0	130.2
			0	1	1	0	0	1	135.8
			0	1	1	0	1	0	142
			0	1	1	0	1	1	148.8
			0	1	1	1	0	0	156.2
			0	1	1	1	0	1	164.5
			0	1	1	1	1	0	173.6
			0	1	1	1	1	1	183.8
			1	0	0	0	0	0	195.3
			1	0	0	0	0	1	201.6
			1	0	0	0	1	0	208.3
			1	0	0	0	1	1	215.5
			1	0	0	1	0	0	223.2
			1	0	0	1	0	1	231.5
			1	0	0	1	1	0	240.4
			1	0	0	1	1	1	250
			1	0	1	0	0	0	260
			1	0	1	0	0	1	271
			1	0	1	0	1	0	284
			1	0	1	0	1	1	297
			1	0	1	1	0	0	312
			1	0	1	1	0	1	328
			1	0	1	1	1	0	347
			1	0	1	1	1	1	367
			1	1	0	0	0	0	390
			1	1	0	0	0	1	416
			1	1	0	0	1	0	446
			1	1	0	0	1	1	480
			1	1	0	1	0	0	521
			1	1	0	1	0	1	568
			1	1	0	1	1	0	625
			1	1	0	1	1	1	Reserved

Table 46. Register 0x41—OUTA Positive Edge Timing (OUTA Pin)

Bit	Name	R/W	Description
[7:0]	t_1	R/W	This register contains the eight MSBs of the 12-bit t_1 time. This value is always used with the top four bits of Register 0x42, which contains the four LSBs of the t_1 time. Each LSB corresponds to 5 ns resolution.

Table 47. Register 0x42—OUTA Positive Edge Setting (OUTA Pin)

Bit	Name	R/W	Description
[7:4]	t_1	R/W	These bits contain the four LSBs of the 12-bit t_1 time. This value is always used with the eight bits of Register 0x41, which contains the eight MSBs of the t_1 time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_1 edge. 0 = no PWM modulation of the t_1 edge.
2	t_1 sign	R/W	1 = positive sign. Increase of PWM modulation moves t_1 right. 0 = negative sign. Increase of PWM modulation moves t_1 left.
[1:0]	Reserved	R/W	Reserved. These bits should be set to 00 for normal operation.

Table 48. Register 0x43—OUTA Negative Edge Timing (OUTA Pin)

Bit	Name	R/W	Description
[7:0]	t_2	R/W	This register contains the eight MSBs of the 12-bit t_2 time. This value is always used with the top four bits of Register 0x44, which contains the four LSBs of the t_2 time. Each LSB corresponds to 5 ns resolution.

Table 49. Register 0x44—OUTA Negative Edge Setting (OUTA Pin)

Bit	Name	R/W	Description
[7:4]	t_2	R/W	These bits contain the four LSBs of the 12-bit t_2 time. This value is always used with the eight bits of Register 0x43, which contains the eight MSBs of the t_2 time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_2 edge. 0 = no PWM modulation of the t_2 edge.
2	t_2 sign	R/W	1 = positive sign. Increase of PWM modulation moves t_2 right. 0 = negative sign. Increase of PWM modulation moves t_2 left.
[1:0]	Reserved	R/W	Reserved. These bits should be set to 00 for normal operation.

Table 50. Register 0x45—OUTB Positive Edge Timing (OUTB Pin)

Bit	Name	R/W	Description
[7:0]	t_3	R/W	This register contains the eight MSBs of the 12-bit t_3 time. This value is always used with the top four bits of Register 0x46, which contains the four LSBs of the t_3 time. Each LSB corresponds to 5 ns resolution.

Table 51. Register 0x46—OUTB Positive Edge Setting (OUTB Pin)

Bit	Name	R/W	Description
[7:4]	t_3	R/W	These bits contain the four LSBs of the 12-bit t_3 time. This value is always used with the eight bits of Register 0x45, which contains the eight MSBs of the t_3 time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_3 edge. 0 = no PWM modulation of the t_3 edge.
2	t_3 sign	R/W	1 = positive sign. Increase of PWM modulation moves t_3 right. 0 = negative sign. Increase of PWM modulation moves t_3 left.
[1:0]	Reserved	R/W	Reserved. These bits should be set to 00 for normal operation.

Table 52. Register 0x47—OUTB Negative Edge Timing (OUTB Pin)

Bit	Name	R/W	Description
[7:0]	t_4	R/W	This register contains the eight MSBs of the 12-bit t_4 time. This value is always used with the top four bits of Register 0x48, which contains the four LSBs of the t_4 time. Each LSB corresponds to 5 ns resolution.

Table 53. Register 0x48—OUTB Negative Edge Setting (OUTB Pin)

Bit	Name	R/W	Description
[7:4]	t_4	R/W	These bits contain the four LSBs of the 12-bit t_4 time. This value is always used with the eight bits of Register 0x47, which contains the eight MSBs of the t_4 time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_4 edge. 0 = no PWM modulation of the t_4 edge.
2	t_4 sign	R/W	1 = positive sign. Increase of PWM modulation moves t_4 right. 0 = negative sign. Increase of PWM modulation moves t_4 left.
[1:0]	Reserved	R/W	Reserved. These bits should be set to 00 for normal operation.

Table 54. Register 0x49—OUTC Positive Edge Timing (OUTC Pin)

Bit	Name	R/W	Description
[7:0]	t_5	R/W	This register contains the eight MSBs of the 12-bit t_5 time. This value is always used with the top four bits of Register 0x4A, which contains the four LSBs of the t_5 time. Each LSB corresponds to 5 ns resolution.

Table 55. Register 0x4A—OUTC Positive Edge Setting (OUTC Pin)

Bit	Name	R/W	Description
[7:4]	t_5	R/W	These bits contain the four LSBs of the 12-bit t_5 time. This value is always used with the eight bits of Register 0x49, which contains the eight MSBs of the t_5 time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_5 edge. 0 = no PWM modulation of the t_5 edge.
2	t_5 sign	R/W	1 = positive sign. Increase of PWM modulation moves t_5 right. 0 = negative sign. Increase of PWM modulation moves t_5 left.
[1:0]	Reserved	R/W	Reserved. These bits should be set to 00 for normal operation.

Table 56. Register 0x4B—OUTC Negative Edge Timing (OUTC Pin)

Bit	Name	R/W	Description
[7:0]	t_6	R/W	This register contains the eight MSBs of the 12-bit t_6 time. This value is always used with the top four bits of Register 0x4C, which contains the four LSBs of the t_6 time. Each LSB corresponds to 5 ns resolution.

Table 57. Register 0x4C—OUTC Negative Edge Setting (OUTC Pin)

Bit	Name	R/W	Description
[7:4]	t_6	R/W	These bits contain the four LSBs of the 12-bit t_6 time. This value is always used with the eight bits of Register 0x4B, which contains the eight MSBs of the t_6 time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_6 edge. 0 = no PWM modulation of the t_6 edge.
2	t_6 sign	R/W	1 = positive sign. Increase of PWM modulation moves t_6 right. 0 = negative sign. Increase of PWM modulation moves t_6 left.
[1:0]	Reserved	R/W	Reserved. These bits should be set to 00 for normal operation.

Table 58. Register 0x4D—OUTD Positive Edge Timing (OUTD Pin)

Bit	Name	R/W	Description
[7:0]	t_7	R/W	This register contains the eight MSBs of the 12-bit t_7 time. This value is always used with the top four bits of Register 0x4E, which contains the four LSBs of the t_7 time. Each LSB corresponds to 5 ns resolution.

Table 59. Register 0x4E—OUTD Positive Edge Setting (OUTD Pin)

Bit	Name	R/W	Description
[7:4]	t_7	R/W	These bits contain the four LSBs of the 12-bit t_7 time. This value is always used with the eight bits of Register 0x4D, which contains the eight MSBs of the t_7 time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_7 edge. 0 = no PWM modulation of the t_7 edge.
2	t_7 sign	R/W	1 = positive sign. Increase of PWM modulation moves t_7 right. 0 = negative sign. Increase of PWM modulation moves t_7 left.
[1:0]	Reserved	R/W	Reserved. These bits should be set to 00 for normal operation.

Table 60. Register 0x4F—OUTD Negative Edge Timing (OUTD Pin)

Bit	Name	R/W	Description
[7:0]	t_8	R/W	This register contains the eight MSBs of the 12-bit t_8 time. This value is always used with the top four bits of Register 0x50, which contains the four LSBs of the t_8 time. Each LSB corresponds to 5 ns resolution.

Table 61. Register 0x50—OUTD Negative Edge Setting (OUTD Pin)

Bit	Name	R/W	Description
[7:4]	t_8	R/W	These bits contain the four LSBs of the 12-bit t_8 time. This value is always used with the eight bits of Register 0x4F, which contains the eight MSBs of the t_8 time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_8 edge. 0 = no PWM modulation of the t_8 edge.
2	t_8 sign	R/W	1 = positive sign. Increase of PWM modulation moves t_8 right. 0 = negative sign. Increase of PWM modulation moves t_8 left.
[1:0]	Reserved	R/W	Reserved. These bits should be set to 00 for normal operation.

Table 62. Register 0x51—SR1 Positive Edge Timing (SR1 Pin)

Bit	Name	R/W	Description
[7:0]	t_9	R/W	This register contains the eight MSBs of the 12-bit t_9 time. This value is always used with the top four bits of Register 0x52, which contains the four LSBs of the t_9 time. Each LSB corresponds to 5 ns resolution.

Table 63. Register 0x52—SR1 Positive Edge Setting (SR1 Pin)

Bit	Name	R/W	Description
[7:4]	t_9	R/W	These bits contain the four LSBs of the 12-bit t_9 time. This value is always used with the eight bits of Register 0x51, which contains the eight MSBs of the t_9 time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_9 edge. 0 = no PWM modulation of the t_9 edge.
2	t_9 sign	R/W	1 = positive sign. Increase of PWM modulation moves t_9 right. 0 = negative sign. Increase of PWM modulation moves t_9 left.
[1:0]	Reserved	R/W	Reserved. These bits should be set to 00 for normal operation.

Table 64. Register 0x53—SR1 Negative Edge Timing (SR1 Pin)

Bit	Name	R/W	Description
[7:0]	t_{10}	R/W	This register contains the eight MSBs of the 12-bit t_{10} time. This value is always used with the top four bits of Register 0x54, which contains the four LSBs of the t_{10} time. Each LSB corresponds to 5 ns resolution.

Table 65. Register 0x54—SR1 Negative Edge Setting (SR1 Pin)

Bit	Name	R/W	Description
[7:4]	t_{10}	R/W	These bits contain the four LSBs of the 12-bit t_{10} time. This value is always used with the eight bits of Register 0x53, which contains the eight MSBs of the t_{10} time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_{10} edge. 0 = no PWM modulation of the t_{10} edge.
2	t_{10} sign	R/W	1 = positive sign. Increase of PWM modulation moves t_{10} right. 0 = negative sign. Increase of PWM modulation moves t_{10} left.
[1:0]	Reserved	R/W	Reserved. These bits should be set to 00 for normal operation.

Table 66. Register 0x55—SR2 Positive Edge Timing (SR2 Pin)

Bit	Name	R/W	Description
[7:0]	t_{11}	R/W	This register contains the eight MSBs of the 12-bit t_{11} time. This value is always used with the top four bits of Register 0x56, which contains the four LSBs of the t_{11} time. Each LSB corresponds to 5 ns resolution.

Table 67. Register 0x56—SR2 Positive Edge Setting (SR2 Pin)

Bit	Name	R/W	Description
[7:4]	t_{11}	R/W	These bits contain the four LSBs of the 12-bit t_{11} time. This value is always used with the eight bits of Register 0x55, which contains the eight MSBs of the t_{11} time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_{11} edge. 0 = no PWM modulation of the t_{11} edge.
2	t_{11} sign	R/W	1 = positive sign. Increase of PWM modulation moves t_{11} right. 0 = negative sign. Increase of PWM modulation moves t_{11} left.
[1:0]	Reserved	R/W	Reserved. These bits should be set to 00 for normal operation.

Table 68. Register 0x57—SR2 Negative Edge Timing (SR2 Pin)

Bit	Name	R/W	Description
[7:0]	t_{12}	R/W	This register contains the eight MSBs of the 12-bit t_{12} time. This value is always used with the top four bits of Register 0x58, which contains the four LSBs of the t_{12} time. Each LSB corresponds to 5 ns resolution.

Table 69. Register 0x58—SR2 Negative Edge Setting (SR2 Pin)

Bit	Name	R/W	Description
[7:4]	t_{12}	R/W	These bits contain the four LSBs of the 12-bit t_{12} time. This value is always used with the eight bits of Register 0x57, which contains the eight MSBs of the t_{12} time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_{12} edge. 0 = no PWM modulation of the t_{12} edge.
2	t_{12} sign	R/W	1 = positive sign. Increase of PWM modulation moves t_{12} right. 0 = negative sign. Increase of PWM modulation moves t_{12} left.
[1:0]	Reserved	R/W	Reserved. These bits should be set to 00 for normal operation.

Table 70. Register 0x59—OUTAUX Positive Edge Timing (OUTAUX Pin)

Bit	Name	R/W	Description
[7:0]	t_{13}	R/W	This register contains the eight MSBs of the 12-bit t_{13} time. This value is always used with the top four bits of Register 0x5A, which contains the four LSBs of the t_{13} time. Each LSB corresponds to 5 ns resolution.

Table 71. Register 0x5A—OUTAUX Positive Edge Setting (OUTAUX Pin)

Bit	Name	R/W	Description
[7:4]	t_{13}	R/W	These bits contain the four LSBs of the 12-bit t_{13} time. This value is always used with the eight bits of Register 0x59, which contains the eight MSBs of the t_{13} time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_{13} edge. 0 = no PWM modulation of the t_{13} edge.
2	t_{13} sign	R/W	1 = positive sign. Increase of PWM modulation moves t_{13} right. 0 = negative sign. Increase of PWM modulation moves t_{13} left.
[1:0]	Reserved	R/W	Reserved. Set these bits to 00 for normal operation.

Table 72. Register 0x5B—OUTAUX Negative Edge Timing (OUTAUX Pin)

Bit	Name	R/W	Description
[7:0]	t_{14}	R/W	This register contains the eight MSBs of the 12-bit t_{14} time. This value is always used with the top four bits of Register 0x5C, which contains the four LSBs of the t_{14} time. Each LSB corresponds to 5 ns resolution.

Table 73. Register 0x5C—OUTAUX Negative Edge Setting (OUTAUX Pin)

Bit	Name	R/W	Description
[7:4]	t_{14}	R/W	These bits contain the four LSBs of the 12-bit t_{14} time. This value is always used with the eight bits of Register 0x5B, which contains the eight MSBs of the t_{14} time. Each LSB corresponds to 5 ns resolution.
3	Modulate enable	R/W	1 = PWM modulation acts on the t_{14} edge. 0 = no PWM modulation of the t_{14} edge.
2	t_{14} sign	R/W	1 = positive sign. Increase of PWM modulation moves t_{14} right. 0 = negative sign. Increase of PWM modulation moves t_{14} left.
1	Regulate with OUTAUX	R/W	1 = control loop PWM modulation is regulated by OUTAUX. The CS1 blanking signal is synchronized with OUTAUX when this bit is set. 0 = control loop PWM modulation is regulated by OUTA, OUTB, OUTC, OUTD, SR1, and SR2 (normal mode).
0	Reserved	R/W	Reserved. Set this bit to 0 for normal operation.

Table 74. Register 0x5D—OUTx and SRx Pin Disable Setting

Bit	Name	R/W	Description
7	OUTAUX disable	R/W	Setting this bit disables the OUTAUX output.
6	SR2 disable	R/W	Setting this bit disables the SR2 output.
5	SR1 disable	R/W	Setting this bit disables the SR1 output.
4	OUTD disable	R/W	Setting this bit disables the OUTD output.
3	OUTC disable	R/W	Setting this bit disables the OUTC output.
2	OUTB disable	R/W	Setting this bit disables the OUTB output.
1	OUTA disable	R/W	Setting this bit disables the OUTA output.
0	GO	W	This bit latches in all registers from Address 0x3F to Address 0x5D. This bit prevents the PWM timing from being temporarily incorrect, if changing PWM timing while the power supply is on.

DIGITAL FILTER PROGRAMMING REGISTERS

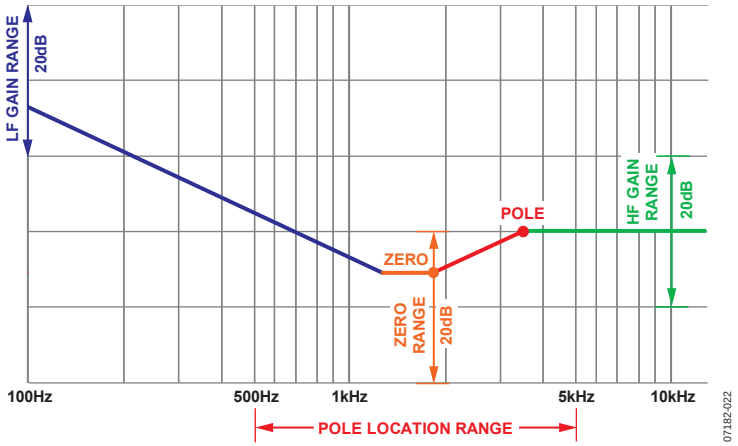

Figure 20. Digital Filter Programmability

Table 75. Register 0x60—Normal Mode Digital Filter LF Gain Setting

Bit	Name	R/W	Description
[7:0]	LF gain setting	R/W	This register determines the low frequency gain of the loop response. Programmable over a 20 dB range. Each LSB corresponds to a 0.3 dB increase. See Figure 20.

Table 76. Register 0x61—Normal Mode Digital Filter Zero Setting

Bit	Name	R/W	Description
[7:0]	Zero setting	R/W	This register determines the position of the final 0. See Figure 20.

Table 77. Register 0x62—Normal Mode Digital Filter Pole Setting

Bit	Name	R/W	Description
[7:0]	Pole location	R/W	This register determines the position of the final pole. See Figure 20.

Table 78. Register 0x63—Normal Mode Digital Filter HF Gain Setting

Bit	Name	R/W	Description
[7:0]	HF gain setting	R/W	This register determines the high frequency gain of the loop response. Programmable over a 20 dB range. Each LSB corresponds to a 0.3 dB increase. See Figure 20.

Table 79. Register 0x68—Password Lock

Bit	Name	R/W	Description
[7:0]	Password	W	This register contains the 8-bit EEPROM lock password. This password is used to protect the register contents from being changed. The EEPROM is always locked. When the EEPROM downloads to RAM, the password is also downloaded. If the user writes the same password to this register, the EEPROM is unlocked and the EEPROM can be updated. After the EEPROM is updated, the EEPROM is locked again.

OUTLINE DIMENSIONS

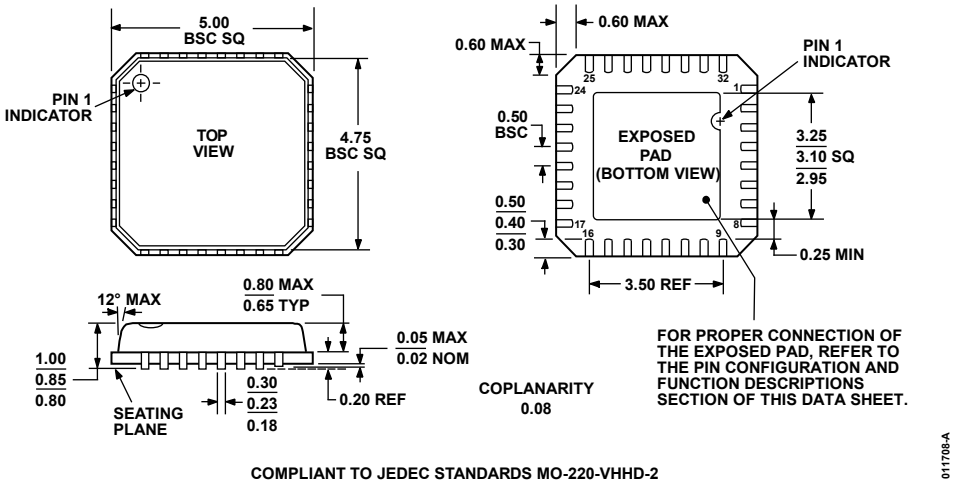

Figure 21. 32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]
5 mm × 5 mm Body, Very Thin Quad
(CP-32-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option
ADP1043ACPZ[1]	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-2
ADP1043ACPZ-RL[1]	−40°C to +85°C	32-Lead Lead Frame Chip Scale Package [LFCSP_VQ]	CP-32-2

[1] Z = RoHS Compliant Part.

NOTES

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